CAHNERS PUBLICATION FEBRUARY 20, 1975

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EDN

CLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

PLL IC's produce a novel AM receiver

Newest μP squeezes 16-bit mini onto a single chip

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There's no such thing as an "Augat-like" contact

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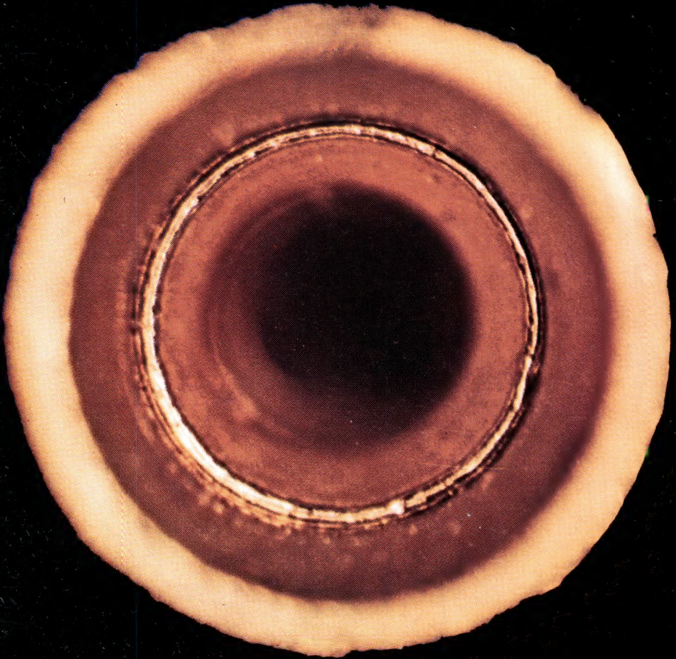

Either it is...

Lots of our competitors call their wire-wrapped packaging panels "Augat-like". But frankly they're not. Because no stamped contact can compare to Augat's machined assembly.

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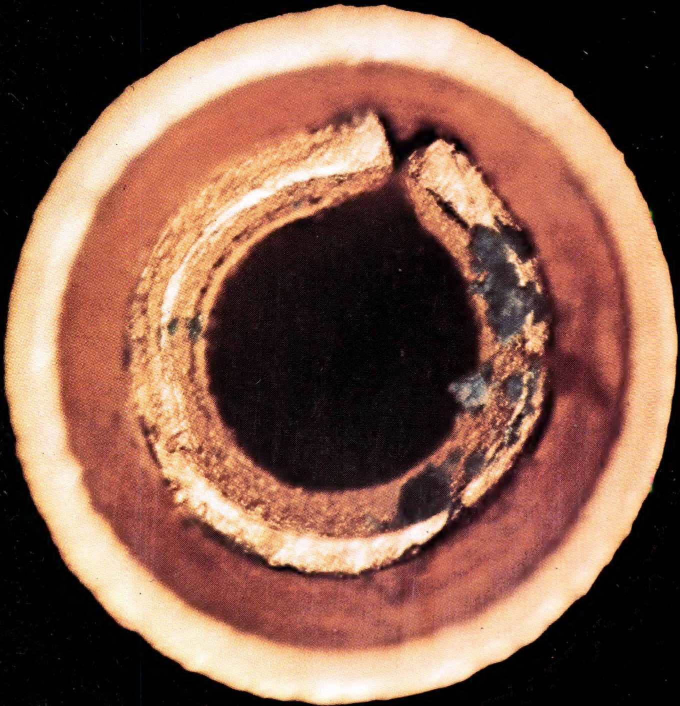
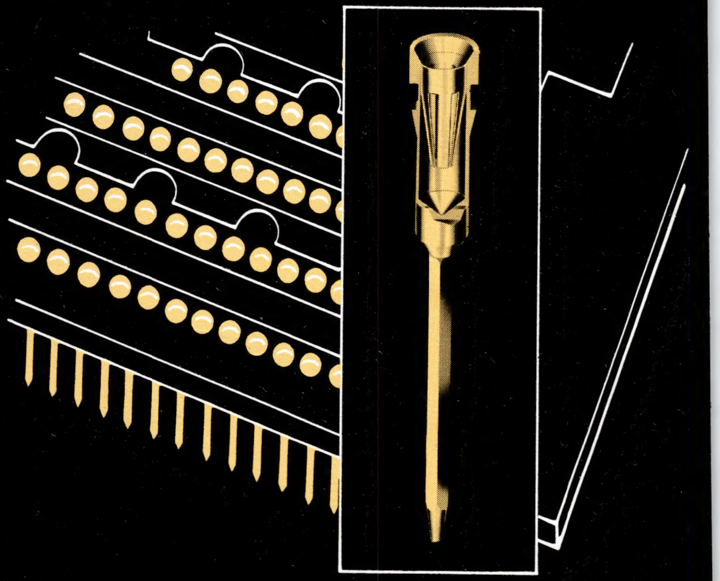
So you see, there is no such thing as an "Augat-like" contact. The closer you look, the more you see why.



or it isn't.



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VOLUME 20, NUMBER 4

EDN

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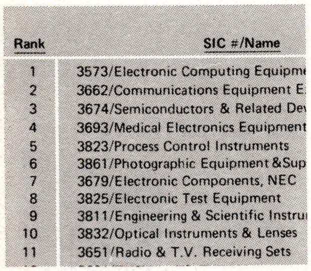

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7	3679/Electronic Components, NEC
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9	3811/Engineering & Scientific Instru
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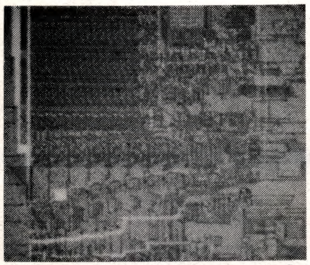

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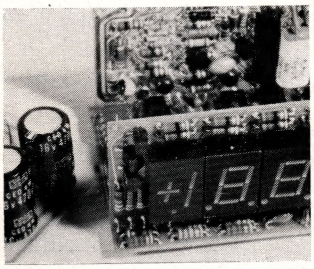

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COVER

Our cover represents a bit of editorial license, because tight industry security prevented us from obtaining a photo of an actual I^{2}L device in time to meet our cover deadline. (See story on pg. 34.) Thus, we are deeply indebted to RCA Solid State Europe for their beautiful shot of a Model MW-7001ID 1k NMOS RAM.

BPA ☆ABP

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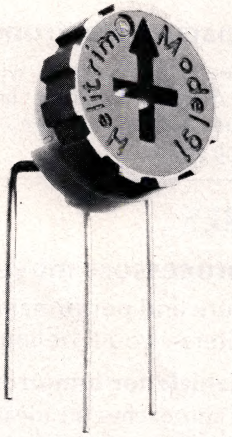
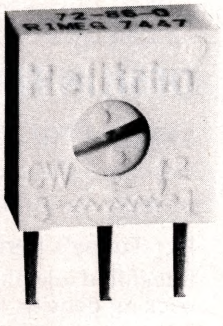
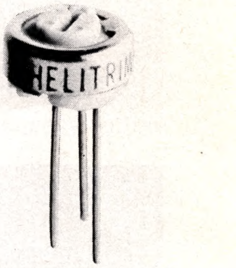
Seven cermet trimmers that







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- 19 resistance values

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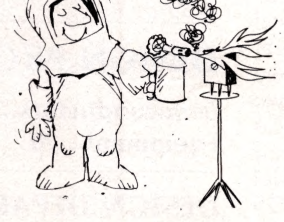

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- Lowest profile trimmer in industry
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- Sealed for board washing
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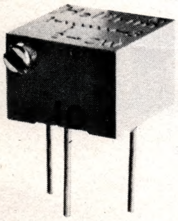

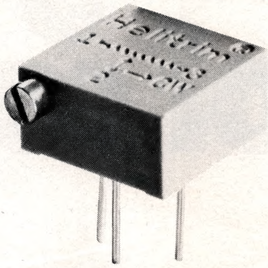

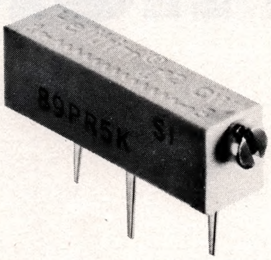

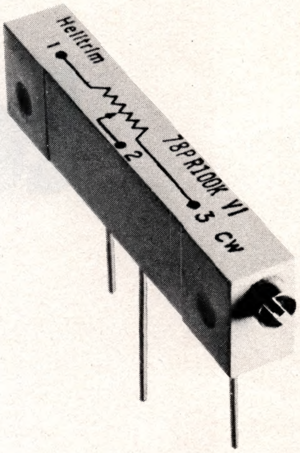

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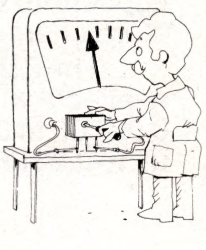

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- 100% inspected

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  - Printed circuit pins
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- Panel mount available
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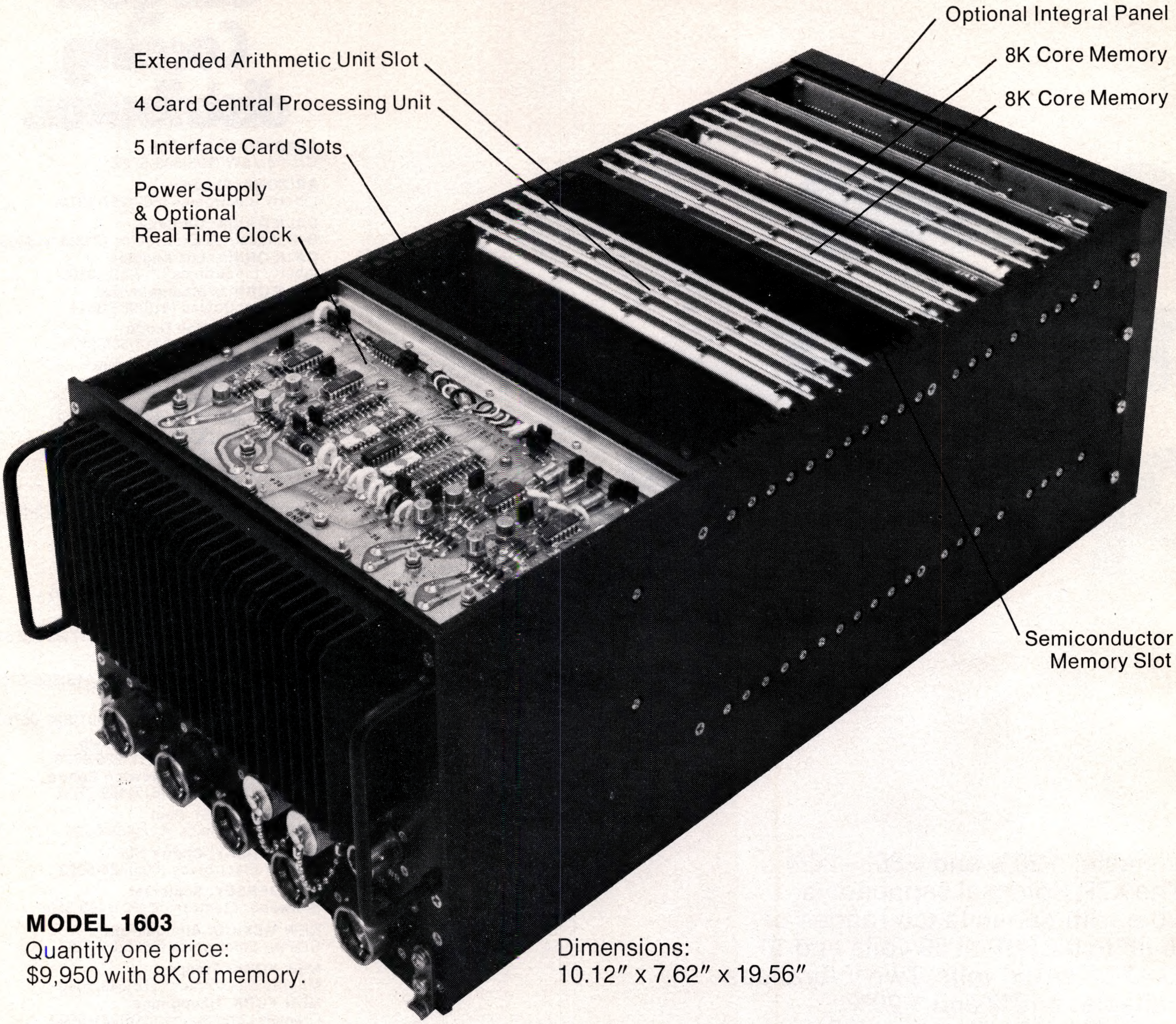
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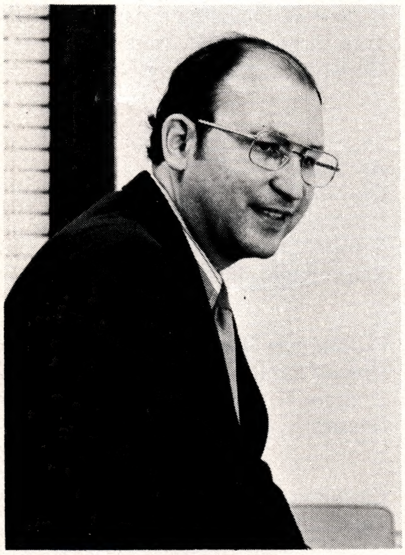
Microprocessors—the ultimate lever?



It's been said many times that the philosophy of major microprocessor manufacturers is to sell their μP's inexpensively and then use them as a lever to sell all the other necessary parts. Since there are many more memory and interface parts to be sold than microprocessors, that's where the largest potential profits are. However, in the absence of collusion, leverage disappears with the advent of a second-source supplier. From then on it's purely competitive.

Until now, the technological significance of available microprocessors overshadowed the lack of second sources. What really concerned the user, as indicated by the EDN Market Study, was performance, availability and vendor reputation. The thing that overcame lack of second sources was the significantly increased performance μP's added to a product without corresponding increases in cost.

Now, something new has been added. It seems as if at least one microprocessor manufacturer is attempting to drive costs up if you don't play the ballgame by his rules. Obviously, as you will see, he is not concerned about reputation.

A friend of mine, working for a local sales representative, came upon the following situation at least three times recently. While attempting to sell IC memories to engineers using one manufacturer's microprocessor, he found them all saying they couldn't buy memory from anyone but that particular μP manufacturer. When asked why, they said that if they did so either the microprocessor's price would be doubled or the μP just wouldn't be supplied.

In the face of such marketing tactics, the apparent cost effectiveness achieved with a particular design can quickly disappear. The total price is no longer determined by the price of individual components chosen for their cost effectiveness, but by a pre-set "package" price. It's quite obvious then that you, the user, can exert little control over this "package" price.

There's nothing wrong with a manufacturer developing companion IC's to go with his μP and then trying to sell an entire package. But it is dead wrong for him to use his microprocessor as a lever to exclude competitive companion IC's.

All is not lost however. You who may be just starting in the μP ballgame have the advantage of at least one second-sourced device as well as the availability of a substantial number of similar devices to choose from. These two things should eliminate the lever and keep things on a competitive plane—if you ask the right questions at the start.

And for those of you already locked into one microprocessor where the leverage situation exists, there's also a solution. The Federal Trade Commission has advised me that if, in fact, competitive memories (or other companion parts) will work properly with the microprocessor, **any manufacturer using his μP as a lever to sell a package is in violation of anti-trust laws.** I urge you to contact the FTC if you fall victim to such tactics. They will take any action necessary to put a stop to this illegal practice.

Roy W. Forsberg

Editor

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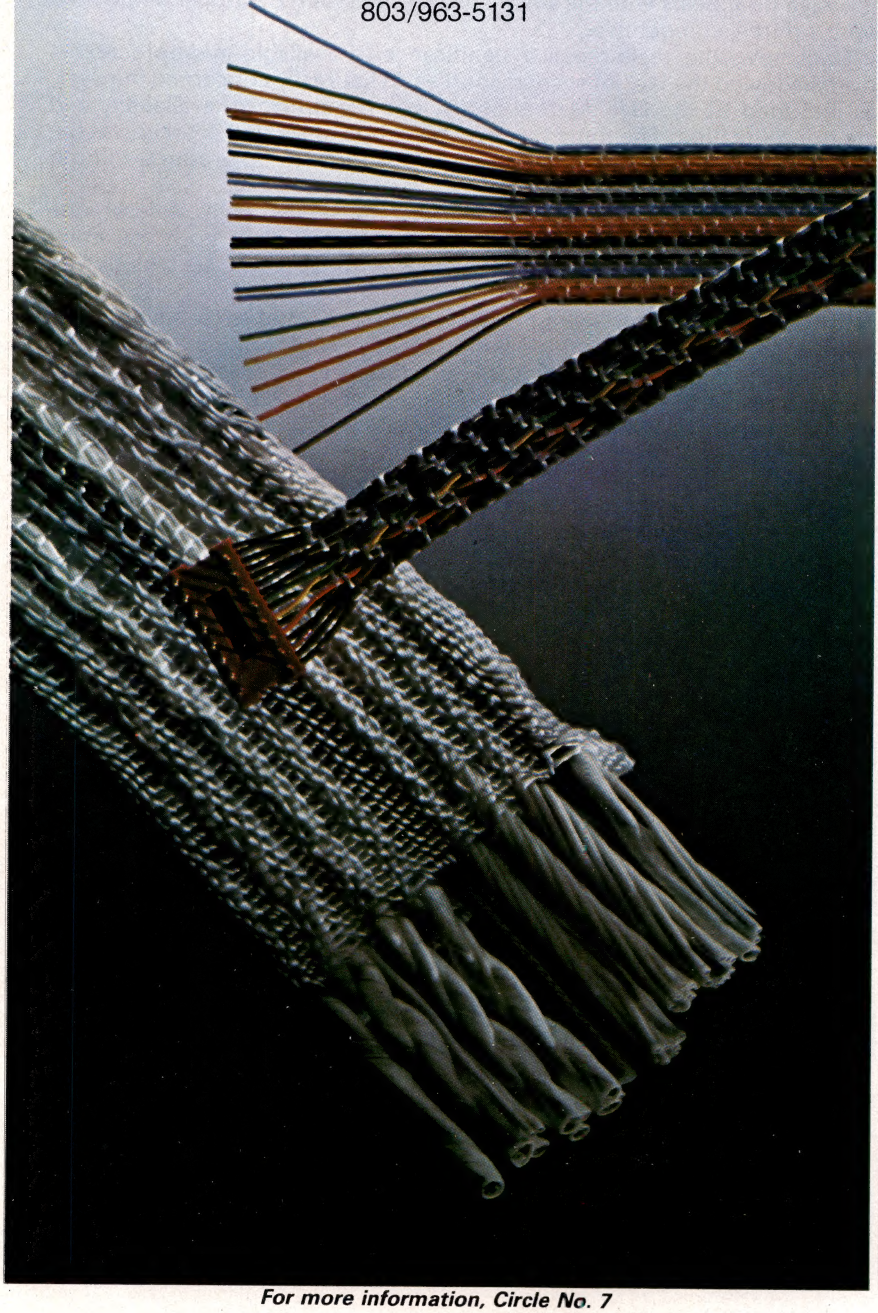

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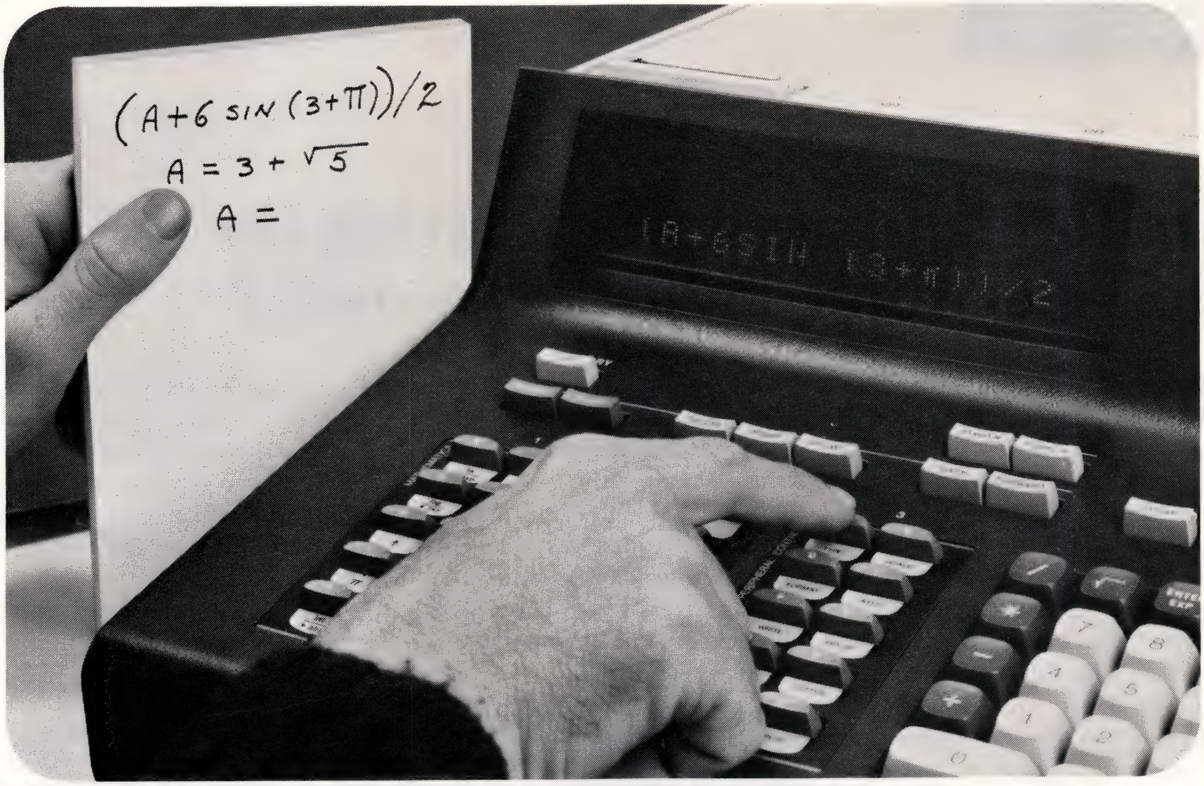

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Are foreign-based firms pacing the U.S. electronic industry's growth?

Electronic related industries have shown tremendous growth over the last 20 years. Most of this growth has been due to the abundance of new products introduced and the profusion of new technology generated during this period.

Which brings up a good question: Because new products often lead to new sales, are those industries (and companies) which generate the most new products the ones which are the most dynamic and fastest growing?

Marketing Development Corp., Concord, MA, thinks so. They believe that a company seeking to find its greatest opportunities in the selection of new products and/or new markets should look at the level of new product activity by industry and/or company. Therefore, M.D. has compiled this information in their "1974-75 Electronics New Product Directory."

Leading the way

Marketing Development's directory lists short descriptions of all significant new electronic products that were introduced by publicly-held companies for their latest fiscal year ending on or before mid-1974. Although many of its results might have been anticipated, it contains a few surprises.

Table 1 shows those electronic market segments which generated the most new products. As such, it supports the theory that one can predict an industry's growth level on its rate of new product development.

One might expect, therefore, that new product activities would also indicate which individual companies are the most dynamic; e.g., the ones likely to show the fastest future growth rates. **Table 2's** surprising conclusion is that the two leading U.S. electronic companies are foreign based.

Perhaps one needs to look at the new product activities over a couple of years to get an even better picture. However, the results for a given year do give a clue as to which companies have been the most aggressive in the short term.

For those interested in the complete story, Marketing Development offers the 300-pg. directory for $300.—*WP*

Rank	SIC #/Name	No. in Category
1	3573/Electronic Computing Equipment	414
2	3662/Communications Equipment Except Telephone	367
3	3674/Semiconductors & Related Devices	184
4	3693/Medical Electronics Equipment	151
5	3823/Process Control Instruments	149
6	3861/Photographic Equipment &Supplies	130
7	3679/Electronic Components, NEC	95
8	3825/Electronic Test Equipment	92
9	3811/Engineering & Scientific Instruments	85
10	3832/Optical Instruments & Lenses	81
11	3651/Radio & T.V. Receiving Sets	80
12	3661/Telephone & Telegraph Apparatus	70
	Other SIC's Related to Electronics Products	602
	Total	2,500

Table 1—Where the action is is indicated by those areas of electronics which introduced the largest number of new products. Data is from Marketing Development's "1974-75 Electronics New Product Directory."

Rank	Company	No. of New Products
1	North American Philips Corp.	35
2	Siemens Corp.	27
3	Beckman Instruments, Inc.	26
4	Honeywell, Inc.	24
5-7	General Instrument Corp.	23
5-7	General Telephone & Electronics Corp.	23
5-7	Tektronix, Inc.	23
8	National Semiconductor Co.	22
9-11	Eastman Kodak Co.	21
9-11	Oak Industries, Inc.	21
9-11	Solid State Scientific, Inc.	21
12	Fairchild Camera & Instrument Corp.	20
13	Raytheon Company	19
14	Varian Associates	19

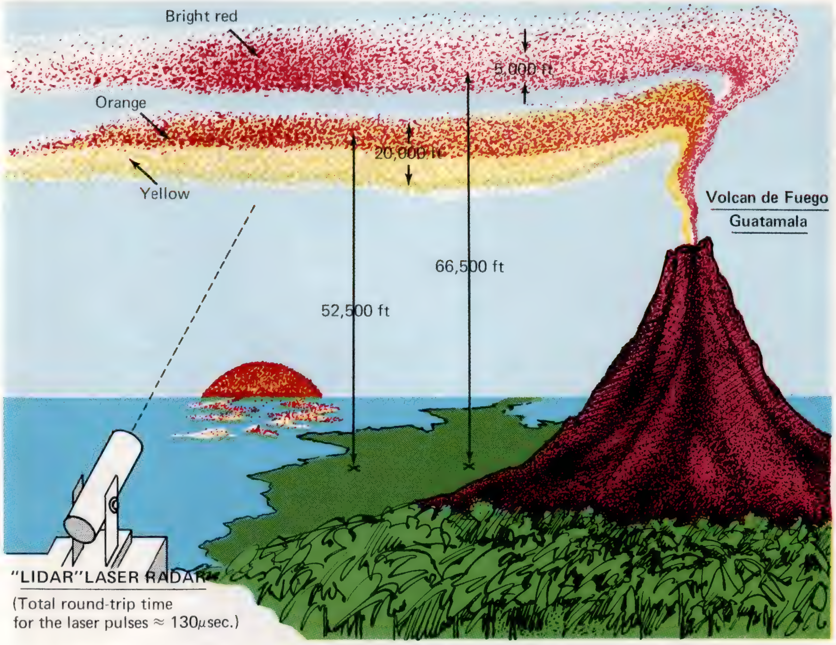
Table 2—Who introduced the greatest number of significant new electronic products for the latest fiscal year ending on or before mid 1974? North American Philips Corp., whose parent company is based in Eindhoven, The Netherlands. Siemens Corp., another European-based company, placed second.

Laser radar connects spectacular sunsets with stratospheric dust

Have you noticed some brilliant, colorful sunsets recently? As strange as it may seem, scientists believe that those beautiful displays were probably caused by the continuing volcanic eruption of Volcan de Fuego in Guatamala.

Dr. Michael P. McCormick and William H. Fuller, Jr. of the NASA Langley Research Center in Hampton, VA reported in the January 1975 issue of Applied Optics the detection by laser radar of two new layers of dust in the stratosphere.

These layers, the scientists claim, were probably formed by the erupting volcano and have now spread over thousands of miles. Sunlight scattering off the stratospheric dust particles produces the vivid effects seen at sunset.



As the sun sets (or rises), its rays are scattered off the stratospheric dust layers from an erupting volcano, producing vivid displays of color. Layers were discovered by Dr. Michael P. McCormick and William H. Fuller, Jr. of the NASA Langley Research Center, Hampton, VA.

Enjoy the brilliant shows

It is still not known exactly when the initial eruption took place. But on November 26, 1974 Dr. McCormick and Mr. Fuller were informed that Professor Aden B. Meinel of the University of Arizona had become aware of it. That same day, the two NASA scientists began making measurements with a laser radar system called lidar. Its ruby laser generates a 100-MW pulse of red light 20 nsec in duration.

They found that 2.7 times as much laser light was scattered back to the earth as when no particles are present in the stratosphere. Then, by measuring the round-trip travel time of the scattered light, the investigators discovered a dust layer 20,000-ft. thick at 52,500 ft. altitude. Another layer 5000-ft. thick was found at an altitude of 66,500 ft.

Since the air in the stratosphere is very stable, it might take as long as several years for the dust layers to dissipate. Thus, beautiful bright red, orange and yellow sunsets could be with us for some time. Moreover, say the scientists, early risers should also view some equally picturesque sunrises.—*WP*

Physicists use Josephson junctions to directly measure laser frequency

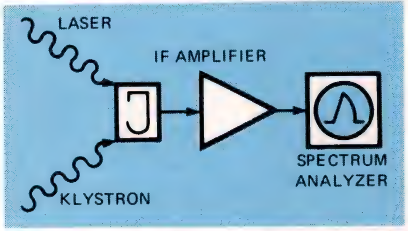
Dramatic moments in the development of physics occur when great synthesis takes place. Perhaps one of the most critical moments happened when J.C. Maxwell combined the laws of electricity and magnetism with the laws of the behavior of light. The resulting study of electromagnetic waves has contributed more to man's understanding of his universe than has any other phenomena because E-M waves can be measured more accurately than anything else.

The most significant recent development in this area comes from National Bureau of Standards' scientists Donald G. McDonald, Alan S. Risley, and John D. Cupp plus Robert J. Ashley, a

Location of a superconducting Josephson junction is indicated by Donald G. McDonald, National Bureau of Standards physicist. The apparatus used at NBS laboratories (Boulder, CO) measures the frequency of infrared radiation, such as that produced by the water-vapor laser shown at the lower right.

Univ. of Colorado electrical engineer. Their development, a revolutionary superconducting generator, uses a Josephson junction. This instrument permits the direct measurement of extremely high frequencies (e.g., the 3800-GHz frequency of an IR laser) with high efficiency and high accuracy.

A possible use for the frequency standard established by this experiment is in earthquake predictions. Detection of extremely slight movements in the earth's crust is now feasible. If such movements can be correlated with quakes, a predictor could be established that would forecast quake possibilities.



Frequency synthesis scheme can be thought of as an infrared heterodyne receiver. It uses the Josephson junction to generate extremely high-order harmonics of the klystron reference and mix them with the applied laser signal. The appropriate beat output is amplified and fed to the spectrum analyzer for frequency measurement.

Higher harmonics are best

To better understand the work of Messrs. McDonald, Risley, Cupp and Ashley, it's necessary to go back to 1972. At that time Dr. Kenneth M. Evenson and colleagues at the NBS Boulder Laboratories amazed the scientific world by accurately measuring the frequency of a helium-neon laser at 88 THz.

This previously unachievable measurement required a battery of six lasers and several steps of harmonic frequency multiplication from the Bureau's primary frequency standard. The break-

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through led to the most accurate value ever measured for the speed of light.

The Evenson experiment used the 12th harmonic of a frequency standard as their basic reference frequency. However, since the most desirable generator for measuring high frequencies is the one producing the highest order useable harmonics, the McDonald group went to work on an improved harmonic generator. Key to their design was a Josephson junction operating at temperatures near absolute zero.

The Josephson junction was chosen as a mixer because theory predicts that as the order of harmonic mixing (n) is increased, the beat frequency current amplitude decreases only slowly (maximum value of $J_n = kn^{-1/3}$). Therefore, very high-order mixing should be observable. Empirical results revealed that n^{-2} power decreases were attainable. The team's success is evidenced by the fact that they used the 401st harmonic of a frequency standard as their reference frequency. In one step, they went from a fundamental of 9.5 GHz to 3800 GHz! Thus they were able to directly measure the frequency of a water-vapor infrared laser.

Upward, ever upward

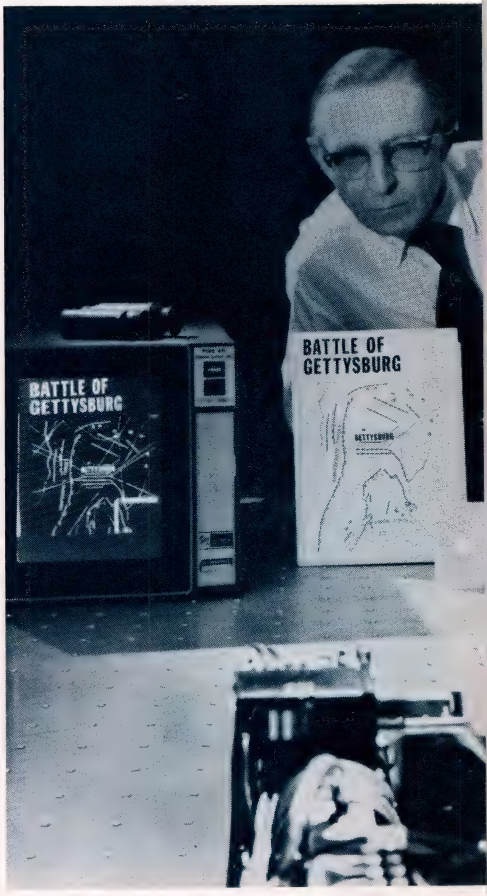
The Josephson junction equipment represents a more efficient way to make very high-frequency measurements. Moreover, it's potentially more accurate than older methods because of the fewer up-conversions required. The project continues with a major rebuild of the equipment currently underway. If successful, improvements will permit the generation of the 1100th harmonic of the X-band source. This, in turn, will extend harmonic mixing to the next higher laser line at 10.7 THz.—*JA*

Semiconductor laser displaces gas type in experimental scanner

For the first time, the feasibility of using tiny, low-power semiconductor lasers to replace bulkier, less efficient gas lasers in an optical scanner has been demonstrated. RCA scientists used a newly developed semiconductor device in a document reader.

While the work is still experimental, the laser has far-reaching implications, according to Dr. George D. Cody, Director of the RCA Physical Electronics Research Laboratory in Princeton, NJ.

Compared with the glass-enclosed gas laser it may replace, the semiconductor laser offers many advantages. In addition to low-drive power and potential low cost, the solid-state device is reliable, rugged, very small, compatible with integrated circuits, and can be modulated easily at high frequencies. Furthermore, it is considered safer than gas lasers, in part because it emits light in the near-infrared region that is less dangerous to the eye.



Invisible, near-infrared light, emitted by a tiny semiconductor laser in the experimental optical scanner in the foreground, "reads" a printed map. Reflected light is detected and processed to produce the image on the CRT. Peter V. Goedertier, a scientist on the RCA team that developed the system, holds a card coated with phosphors that glow when struck by the laser beam.

Checking out the checkouts

Dr. Istvan Gorog headed the RCA team that developed the new document reader. Other members were Peter V. Goedertier, Dr. Joseph D. Knox, Ivan Ladany, and Dr. James P. Wittke.

The solid-state (injection) laser they used is a small chip of specially fabricated and doped aluminum-gallium arsenide. It provides a continuous, astigmatic beam of near-infrared light about 8000 Angstroms.

Optically shaped in the document reader to a nearly round cross section, the laser beam is scanned over the document being read. Galvanometer-driven mirrors control the horizontal and vertical direction. The experimental system detects the reflected laser light, processes it, and then displays the result on a CRT.

Power required to drive the laser is about 1W, compared with up to 10W needed for a gas laser. Output of the injection laser is ≈10 mW, while beam power onto the document is about 3 mW.

The reader scans an 8-in. horizontal line in 12 msec, providing 2000 spots/line resolution. It takes 14 seconds to complete the vertical scan of a 10-in. long document.

According to Dr. Cody, several prospective applications exist for scanners using solid-state lasers. One of the most promising is in automated checkout equipment presently being introduced in supermarkets. Other potential uses are for facsimile equipment and for reading information from optical discs containing video or computer memory information.-*WP*

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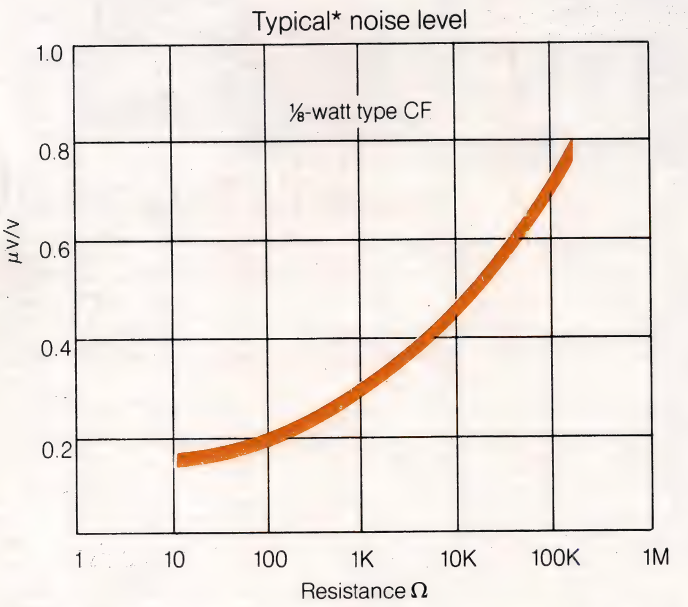
New economical ⅛-watt carbon film resistor



*"Typical" is defined as the maximum value of measurement unit to be expected in 95% of the population of a distribution.

We have the most advanced space-saving ⅛-watt carbon film resistor—a superior replacement for the RC 05—and we'd be delighted to send you samples.

Electrical noise is exceptionally low and is typically less than −20 DB at 10 ohms to −4 DB at 220 K ohms, based on 1μ volt of noise per volt equal to 0 DB.

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Dielectric strength of the jacket is 500 volts RMS.

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Flame retardant coating is another feature of this resistor. Available from 2.2 ohms to 220 K ohms, 5% standard tolerance.

Mechanically interchangeable with both composition and metal oxide resistors of the same wattage. The resistor is only 0.071 inches (1.8mm) in diameter and 0.177 inches (4.5mm) long, maximum.

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HOW TO BUY OEM COMPUTERS WITHOUT BEING EATEN ALIVE.

Part II of ComputerAutomation's OEM Survival System

Continuing the saga of OEM-unique hardware, software, and support vs. the Minivores. And now the Microvores, too.

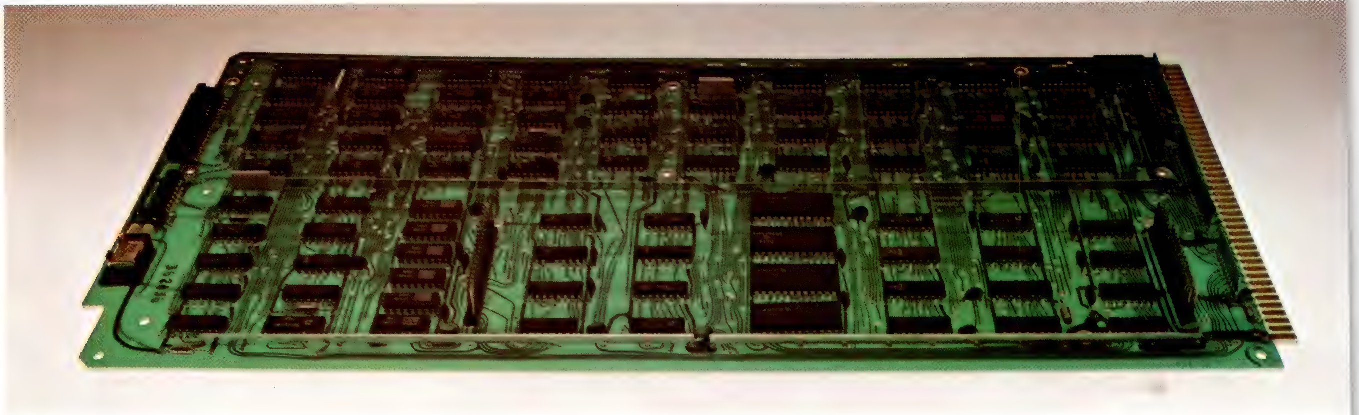
Because the world of product computerization remains a jungle. A dense tangle of conflicting computer claims filled with awful consequences for the unwary. Like getting to market last. Like being priced out of it once you do get there. Like explaining where the profits went. Like unemployment.

In other words, like being eaten alive.

Part I of CA's OEM SURVIVAL SYSTEM offered some crucial insights into the OEM predicament — especially in the area of post-sale support. If you missed this classic Minivore manifesto, send for your copy now.

Next, watch for Part III of the jungle jeopardy: what an OEM needs to know about software to keep from being eaten alive.

Introducing the Naked Milli:™ the world's first millicomputer.



Meet the Milli.

Nature abhors a vacuum. So naturally something eventually comes along to fill it.

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Plus a lot more I/O — three standard I/O systems that even include Direct Memory Access for really high-speed applications.

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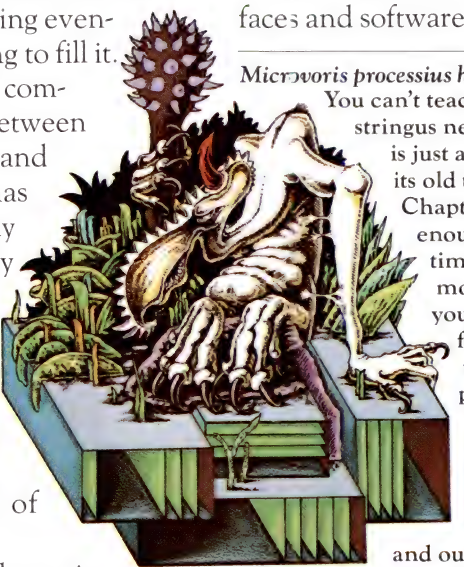
Naturally, the NAKED MILLI is program compatible with our NAKED MINI® machines. Which instantly gives you a broad choice of memories, interfaces and software.



Microvoris processius hamstringus

You can't teach an old hamstringus new tricks. Which is just as well, because its old tricks (see Chapter XI) are bad enough. So each time you need a bit more capability, you have to start from scratch with a bigger processor, all new interfaces, and brand new software. Or go with the NAKED MILLI and our guarantee that if you outgrow it, you can move up to a completely compatible NAKED MINI using the same software, I/O, and interfaces.

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Ask a simple question, and you get a simple answer. And as long as you keep it that way, a microprocessor should work out just fine.

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Problems have a way of growing on you. So before you start beating the bushes for a microcomputer, look at our millicomputer. Power. Price. Open-ended growth.

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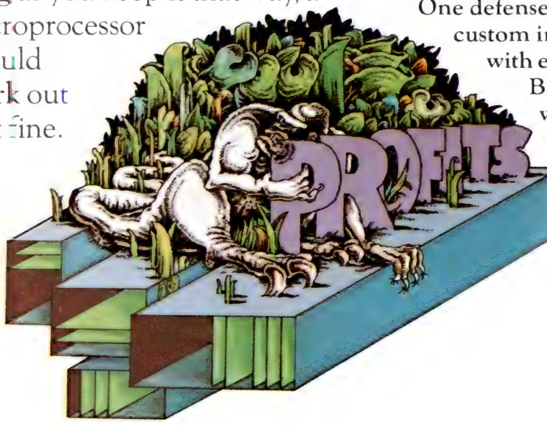

Microvoris computus moronicus (a suborder of Stuntus retardus)

Dumb but dangerous. Once this witless wonder figures out he can put the bite on your budget, he'll gnaw your profits down to the bare bones. One defense is to surround him with custom interfaces and dazzle him with expensive programming. Better yet, outsmart him with our NAKED MILLI. It's got the I.Q. to see to your revenue.

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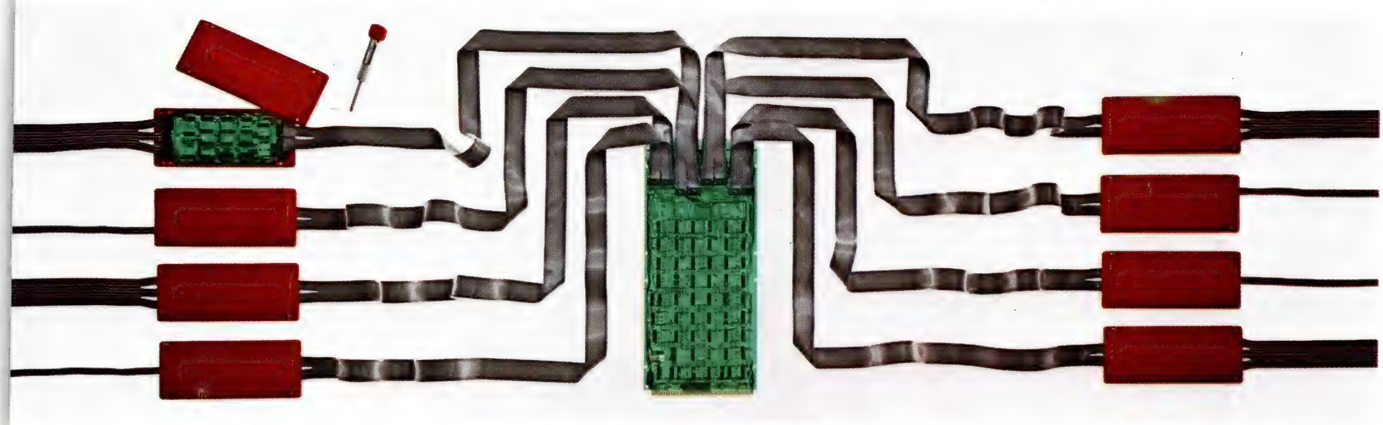

Mother's little helpers.

Necessity is still the Mother of Invention. But as it turns out, ComputerAutomation is the only OEM supplier who's giving Mom a hand.

This time it's interface hardware. Our new truly low-cost Distributed I/O System.

Getting I/O cost down was a necessity, because while the cost of processors and memories has been decreasing, the cost of interface hardware has been standing still.

End users wouldn't appreciate that problem. Nor would their suppliers. But for OEM's it's a very real cost factor, and we understand.

A board in the hand is worth eight Microvores in the bush.

That's how it works out. With our Distributed I/O System you get a choice of up to 8 interfaces — all built into one compact package. All for a lot less than you could possibly design and build it for yourself.

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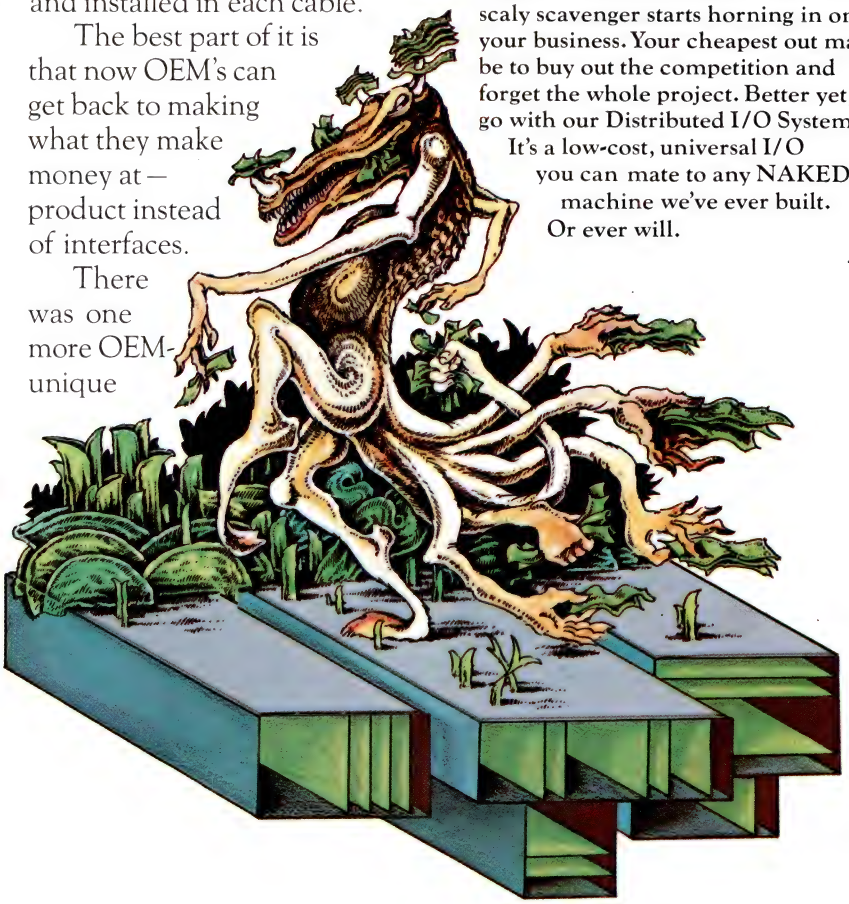
The best part of it is that now OEM's can get back to making what they make money at — product instead of interfaces.

There was one more OEM-unique necessity that we worried about along the way: OEM's sometimes switch machines somewhere downstream. So, ideally our new Distributed I/O System should fit all our machines — from the NAKED MILLI on up.

It does. And that's the Naked truth.



Microvoris interfacii bankruptus

Look out for your ledgers when this scaly scavenger starts horning in on your business. Your cheapest out may be to buy out the competition and forget the whole project. Better yet, go with our Distributed I/O System. It's a low-cost, universal I/O you can mate to any NAKED machine we've ever built. Or ever will.

Introducing the MegaByter™ and the widest range of compatible computers in the world.

Pardon our humility.

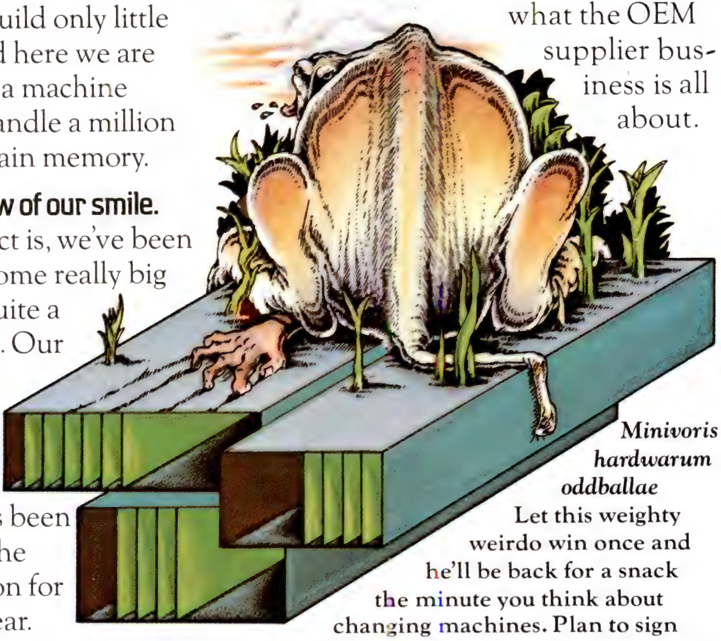
Could be our almost new MegaByter (we've already delivered 15) will alter a lot of people's perspective about us. After all, we're the company who's supposed to build only little minis. And here we are delivering a machine that can handle a million bytes of main memory.

The shadow of our smile.

The fact is, we've been building some really big stuff for quite a long while. Our NAKED MINI LSI 2/20, for instance, has been eclipsing the competition for nearly a year.

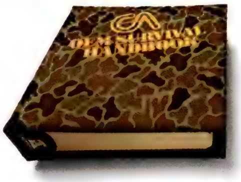
And our new MegaByter is even bigger: 224 dynamite instructions including 31-digit decimal arithmetic, multiple hardware stacks, text string move and compare, (etc$_1$, etc$_2$ . . . etc$_{200}$). All of which adds up to shorter programs that use less memory and run faster.

So obviously it saves OEM's a lot of dough. And unless we've been seriously misinformed, that's what the OEM supplier business is all about.



Minivoris hardwarum oddballae

Let this weighty weirdo win once and he'll be back for a snack the minute you think about changing machines. Plan to sign on plenty of plump project personnel. Or, better yet, keep him starved for attention by computerizing with our totally compatible family of NAKED MILLI and NAKED MINI machines.



The same kind of cost-saving logic is designed into all of our machines, from our new NAKED MILLI all the way up to the MegaByter: build it better; build it for less.

Minimizing the Minivores.

There are a lot of other ways we cut costs for the OEM. By building only program-compatible machines, for instance.

That way, if and when a bigger or smaller machine is called for, you can switch rather than fight. All your original programming, I/O, and interface hardware will work just as well as they ever did. Which means you'll be thousands of dollars ahead of the game. And months ahead on your schedule.

Okay, so maybe we're not humble. At least we're understanding.

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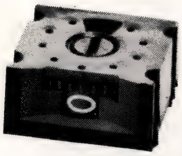

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Single-chip microprocessors move into the 16-bit arena

Compare the architecture and performance of this 16-bit µP against the best of modern minicomputers—you'll be impressed.

Robert H. Cushman, Special Features Editor

It seems only a few months ago that microprocessor designers told us they could not see µP CPU's going over 8-bit wide data words (**Ref. 1**). There just wasn't enough room to carry 16-bit wide data buses around on a reasonable-sized chip.

Well, nothing seems to stop the dizzy speed of µP progress, and now we find that there are at least two single-chip CPU µP's available with 16-bit wide data paths. One is the National PACE, a chip photo of which was shown in a past issue (**Ref. 2**). The other, which we'll look at in this article, is General Instrument's CP-1600 (**Fig. 1**).

National's PACE went to the full extreme of having a 16-bit wide ALU. GI's CP-1600 has only an 8-bit wide ALU, but—as will be seen—halfwords or 8-bit bytes are pipelined through so adroitly that a user can't complain that this compromise slows down the processor. The CP-1600, with its 100-nsec gate clocking, appears as a fast 16-bit machine on the outside.

The µP system that DEC is developing from Western Digital's 3-chip CPU will be even more powerful. DEC sources say it will handle the instruction set of the middle-of-the-line PDP-11/40 model, and its speed will be faster than the bottom-of-the-line PDP-11/05. But with a 3-chip CPU and considerably more external TTL support logic, it will, perforce, be a more expensive system than the single-chip CP-1600 and PACE systems.

The man behind the CP-1600

The CP-1600 is Jeff Stein's baby. Since nearly a year ago, Jeff has managed the CP-1600 program at General Instrument Corp., Hicksville, NY. However, his history with the CP-1600 goes back to the chip's beginning because Jeff was formerly with the sponsoring customer for the CP-1600, a well-known manufacturer of industrial process controls.

His mission was to develop the specifications for a process-control computer that could be implemented in MOS/LSI. "We found we had to have a fairly powerful and fast 16-bit machine," Jeff says. "You need a 16-bit word to handle the data produced by A/D converters (15 bits plus sign); you also need computing power because the control algorithms involve a lot of multiplication, division and square-root computation; and you need speed because, in replacing analog controllers, the computer is expected to go through the control algorithm three times a second."

"Our plans were pretty ambitious from the start. Back in '71 my group realized that we had to have a machine of the caliber of the PDP-11's. It is poor economy, in my opinion, to skimp on the machine and then drive up the user's programming costs, especially in the industrial control field where many custom variations in end equipment will be required. Therefore, I wanted the CP-1600 to have the latest third-generation architecture. At the same time I was convinced that the entire CPU had to be on one chip, because we wanted to be able to substitute these all over the place as replacements for analog controllers. And the price had to be low."

The new architecture

What is meant by the "new architecture"? According to Bill Sweet of Interdata (a minimaker claiming to be a leader in adopting the new architecture), the essential ingredient in a progressive new third-generation machine is an abundance of general-purpose registers in the CPU. These registers give the programmer a choice of data paths through the CPU and let him bypass the traffic jams that so often occur with older, simpler architectures.

The primitive PDP-8 has only one accumulator, and the poor programmer must single-file all data movements through this bottleneck (the accumulator is a fixed, implied address in practically every instruction). Second-generation mini's, like the Nova's, Varian and HP machines, etc., open up the data path a bit for the programmer by throwing in a second accumulator, and perhaps an index register or two. But in contrast, third-

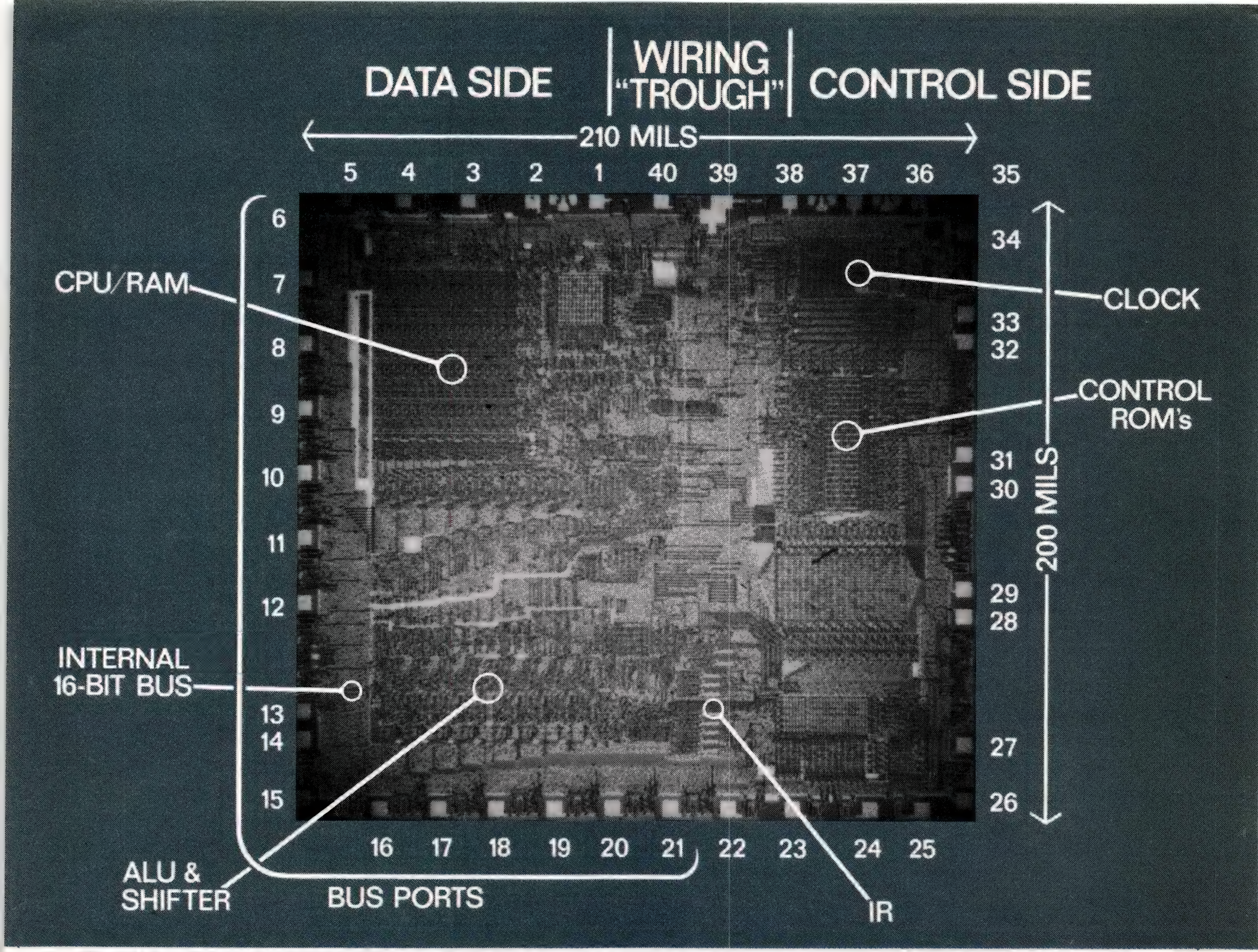


Fig. 1—The CP-1600 CPU chip is laid out so logically that you can practically figure out how it works just by examining it under a magnifying glass. The data side is on the **left**. It contains the RAM that houses the GP registers and the ALU. Then there is the control side on the **right** that takes the clock inputs and instruction register (IR) inputs and produces the control signals for the data side in a sequence of ROM's. In between is the "trough" area which carries the commands and status feedback signals between the two sides. Note how the layout keeps the 16-bit bus quite short.

generation machines, like the Interdata models and DEC PDP-11's, have at least a half dozen general registers that can be software-assigned as individually addressed accumulators, index registers, or whatever, at the programmer's option. The op codes for these third-generation machines have special bits that allow the programmer to make these assignments as he writes the instruction. (In fact, a study of the op codes is often the best way to determine just how "new" the architecture of a machine is.)

In EDN's analysis, the CP-1600 does not fully meet the "new architecture" goal because of some specialization and limitations in the generality of the eight CPU registers. However, the CP-1600 approaches the goal closer than most microprocessors. Part of this is due to the particular way it carries all its CPU registers in one common RAM so it can address and route any one of them as easily as the other.

This, incidentally, is a good example of how MOS/LSI seems to be helping μP's incorporate the best features of top-of-the-line minicomputers. Matching minicomputer speed may always remain a problem for MOS μP's, but it now looks like they will have no trouble in surpassing the architectures of all mini's (and medium-scale computers).

System configuration

An unavoidable compromise you must make when you squeeze a 16-bit CPU into a 40-pin DIP package is moving both data and addresses in and out of the CPU on the same 16-bit bus. You can't have the separate address and data buses that have become standard in 8-bit machines. This doesn't necessarily cost you operating speed because rarely would the address and data flow at the same time in a computer (you always have to set up the address prior to moving the data), but it does cost you extra parts for latching.

Fig. 2 shows the extra system complexity. An address bus latch (two 9308's) is used to take the address bits off the main 16-bit bus and hold them on the externally-created address bus. Extra control signals for this latch and other external functions are provided by the demultiplexer (DM74145) that generates eight external controls from just three CPU pins. Finally, as these external elements need timing information, some flip-flop counters are added to the clock circuit to externally generate the TS-1 and TS-4 time slot strobes. These strobes are available internally in the CPU but there are no pins left to get access to them.

The need for these additional parts ought not to concern the user of a 16-bit microprocessor as much as the user of an 8-bit one. The very fact that the application calls for a 16-bit word probably will involve a fair amount of memory and I/O. Therefore, the chance exists that no MOS CPU would be capable of driving the external system lines without help from bipolar buffers anyway. These external latches and decoders also provide buffering, and in fact, Jeff chose those called out because of their healthy drive capabilities. For example, rather than using just an ordinary TTL 7442 4:10 decoder, Jeff shows a 74145 that has generous 80-mA drive capability.

The alert reader will note a group of "EBCO" outputs and one "EBCI" input coming out in parallel with the data bus. These unorthodox I/O lines were put in specifically for real-time control monitoring of alarm points and limit switches, etc. As shown in **Fig. 2**, the outputs are externally demultiplexed into 16 lines. The CP-1600 has a special instruction (BEXT) that contains bits to select one of these 16 points for query. The response will come back on the ECBI input, which is wired to all the points.

These external sense lines provide a fast and efficient way for the CP-1600 to periodically check plant alarms. It's better than using the interrupt—which the CP-1600, of course, also has—for it will give a positive log of "all's well" for these external points (to prove that the wiring to the alarm is intact, for example). The BEXT instruction incorporates a conditional branch so that if the alarm happens to be set, then the BEXT will branch the CP-1600 program immediately to the proper service subroutine for that point.

A logical chip layout

The CP-1600 CPU chip purposely is partitioned into two distinct sides, as can be seen in **Fig. 1**. There is the data side (**left**) containing the general registers in a RAM array, the ALU, and the internal 16-bit data bus and the 16 ports to the outside world. Then there is the control side (**right**) containing the ROM's to decode the instructions and generate the appropriate detailed commands that will cause the data side to execute the instructions.

Jeff explained: "We purposely kept the two sides separate so we could handle them as independent subsystems. Although we don't intend our machine to be custom microprogrammable, we can change the personality of the chip rather easily by changing the control ROM's and the wiring in the middle "trough" area that connects the two sides. This is why we will be able to bring out an 8-bit version of the CP-1600 chip—the CP800—later this year."

We see more and more microprocessor makers taking a similar "evolutionary" attitude toward their large investment in new CPU chips. Like GI, they plan to get added mileage out of the initial chip with subsequent variations. But GI is the first to tell us they have the elements of their CPU chip set up on an automated layout system. Thus their artwork computer (still a Nova minicomputer) will help them do modifications of the CP-1600 chip. Apparently, GI has used this approach for some time in turning out new calculator chip models, all based on the same initial chip design.

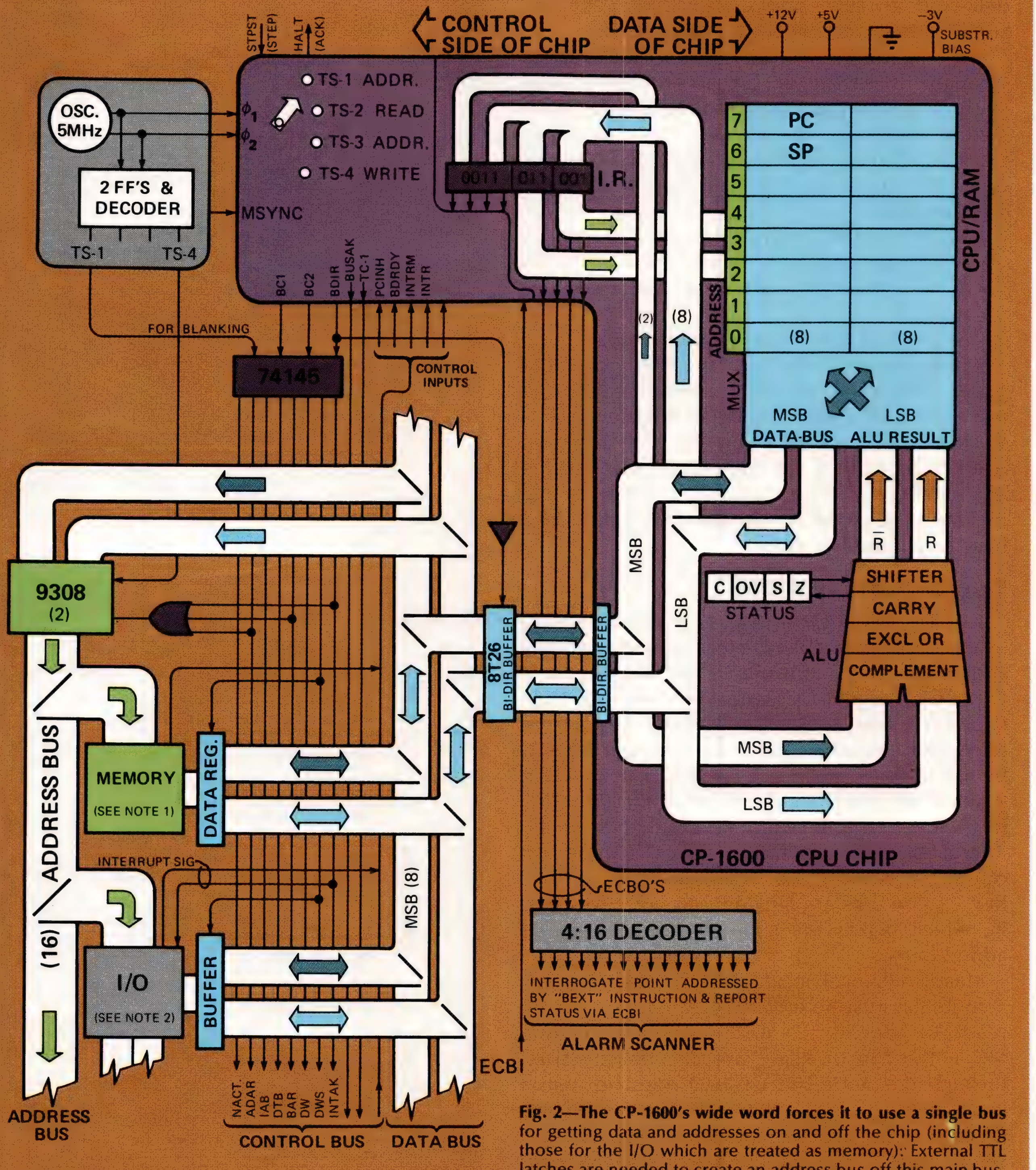
Large-volume μP users ought to keep this in mind, for it probably means they could talk GI into making custom modifications. Jeff grudgingly agreed: "I'm totally against bothering with custom microprogramming, but if a customer promised he'd use 100k units a year and asked us for a reasonable modification, I guess we'd have to listen."

CPU data flow

The CPU chip's data-handling mechanics give one a great deal of insight into the "personality" of the CP-1600. The data side of the CPU is built around a special RAM array whose cells can be doubly addressed. This produces a very natural and efficient flow of data onto the 16-bit wide internal data bus and through the 8-bit wide ALU.

Jeff invented the doubly-addressed RAM back in 1971. As shown in **Fig. 3a**, it is a variation of the standard static RAM. The two cell readout gates, A and B, that are normally controlled by the same address line, are now individually controlled by two separate address lines, A and B. The A side reads out the TRUE value of the cell, and an inverter on the B side sense line makes it also read out the TRUE value.

Fig. 3b shows how one register, Reg 0, could be read out via its A side while another register, Reg 2, could be simultaneously read out via its B side. Thanks to the 16-bit wide bus, the two halfwords (8-bit bytes) from this dual readout can be



NOTES:
1– 10-BIT ROM UNDER DEVELOPMENT TO MATCH IR.
2– I/O "μP" WITH OWN INSTRUCTION SET (PIC 840/850) UNDER DEVELOPMENT.
3– SEE MFGS DATA FOR DETAILS ON CONTROL SIGNALS

Fig. 2—The CP-1600's wide word forces it to use a single bus for getting data and addresses on and off the chip (including those for the I/O which are treated as memory): External TTL latches are needed to create an address bus off this main bus, and these external latches in turn require more controls from the main CPU chip. However, in the more ambitious applications where a designer would turn to a 16-bit machine, these external parts would probably be insignificant compared to the memory and I/O chips. Furthermore, the systems user would probably welcome the additional access to CPU controls.

presented to the 8-bit wide ALU simultaneously. Or, a full-width 16-bit word can be read out onto the bus and delivered to the 16 off-chip drivers, as indicated in **Fig. 3c**. Additional addressing lines select most significant bytes (MSB's) and least significant bytes (LSB's).

The RAM cells need push-pull action from both sides during a write operation, but this is also provided by the CP-1600 CPU chip architecture. The eight outputs of the 8-bit wide ALU are delivered as TRUE and COMPLEMENT on the 16-bit wide bus to the RAM's write ports.

The manner in which the CP-1600 cycles through its ADDR or register-to-register add instruction will show how neatly the CPU architecture falls together (**Fig. 4**). This instruction takes six CP-1600 cycles or 2.4 μsec. Each 400-nsec cycle consists of four 100-nsec time slots of the 4-phase clock:

- At TS-1 the CPU RAM is addressed for read.
- At TS-2 the CPU RAM is read out.
- At TS-3 the CPU RAM is addressed for write.
- At TS-4 the CPU RAM is written into.

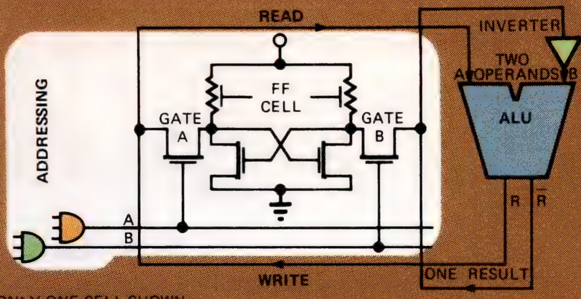
Jeff is proud of the way this data movement pattern keeps the ALU busy most of the time and makes its 8-bit width invisible to the user. As **Fig. 4** shows, the bytes from the RAM are so overlapped as they are "pipelined" through the ALU, that the MSB's are actually starting through the first stage of the 4-stage ALU before the LSB's have exited the last stage.

The six cycles of ADDR

The first microcycle, MC-1, is the inevitable instruction fetch. GP register 7 is automatically addressed by the control side for this step, as is the PC (Program Counter) in the CP-1600. (However, that doesn't prevent the Reg 7 from also being addressed and manipulated in the ALU by the very instructions it fetches. This makes it easy to do program jumps with the CP-1600.) Reg 7 is sent out full width (LSB and MSB) on the internal bus in MC-1. In time-slot 3 (TS-3) it is sent out to the external bus. There, in MC-2, at TS-1, Reg 7's contents are latched into the 9308's (**Fig. 2**), which makes the contents available to the address bus.

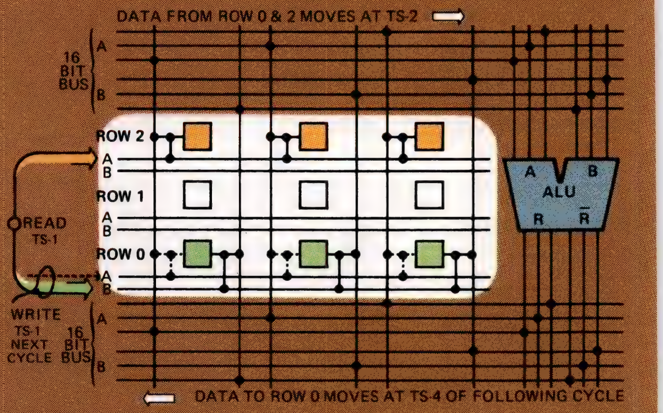
Meanwhile, back inside the CPU, the PC or Reg 7 contents must be incremented so they will be ready to address the next instruction. During MC-1, the LSB of Reg 7 was also being started through the ALU. The CP-1600 does not use a local special-purpose incrementer for its PC, as do most of the μP's we have discussed so far, but sends the PC through the same ALU that processes regular data for incrementation. The ALU consists of four stages as shown, so it takes four 100-nsec time slots to process data through it. "In this case the LSB of Reg 7 is the only data coming into the ALU, and the +1 is added to the LSB by the circuit expedient of forcing the ALU carry to ONE," Jeff said.

The MSB of the PC is processed by having the Reg 7 readdressed in MC-2, but with the readout circuits switched causing the MSB of Reg 7 to be put onto the LSB side of the 16-bit internal bus. This insures that the PC's MSB goes to the proper



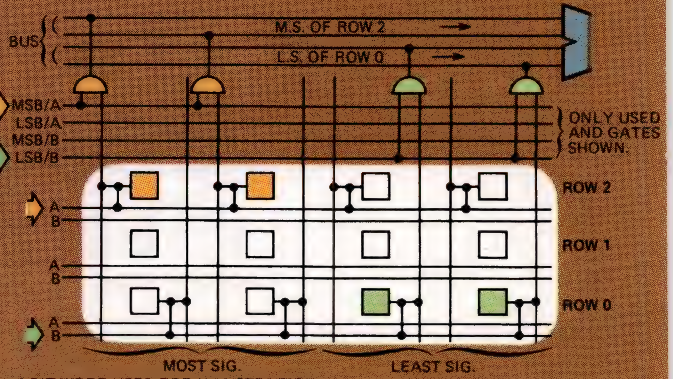
ONLY ONE CELL SHOWN

Fig. 3a—Starting point for the CPU design was this doubly-addressed and read-out RAM. A variation on the familiar static RAM cells, it permits the two operands typically needed by the ALU to be addressed and read out simultaneously. The two gates, A and B, on either side of the storage cell flip-flop are addressed by separate lines—also labelled A and B. The A side will read out the TRUE value of the cell, and the B side will read out the complement, but the inverter in the B output makes both sides TRUE.


DATA FROM ROW 0 & 2 MOVES AT TS-2
16
BIT
BUS
A
B
ROW 2
ROW 1
ROW 0
READ
TS-1
WRITE
TS-1
NEXT
CYCLE
16
BIT
BUS
ALU
R
R̄
DATA TO ROW 0 MOVES AT TS-4 OF FOLLOWING CYCLE

3-BIT WORD USED FOR ILLUSTRATION

Fig. 3b—How two different registers (rows) can be simultaneously read out of the CPU/RAM. This happens during the first two time slots (TS-1 and TS-2) of the CPU "microcycle." Each time slot is 100 nsec long and represents the time needed to switch one stage of logic gates. The last two time slots (TS-3 and TS-4) are used to write the results back into the CPU/RAM, but because the 4-stage ALU itself takes 400 nsec, this can't be done until the next microcycle. However, note that only one register can be written back at a time, as it takes both a true and a complement drive signal to write back into these cells.



4-BIT WORD USED FOR ILLUSTRATION

Fig. 3c—How either 8-bit byte of the 16-bit words can be fed to the 8-bit ALU ports via selective I/O multiplexing of the CPU/RAM. This allows the RAM to either deliver a full 16-bit register to the 16-bit bus for off-chip operations, or to deliver pairs of bytes or halfwords to the 8-bit ALU during on-chip computations. Actually, to conserve chip area, the read and write operations are combined in a single MUX at the bottom end of the RAM.

side of the ALU for incrementation. It will only be incremented if there is a carry left over from the LSB.

As can be seen from a study of MC-2 in **Fig. 4**, the MSB starts into the first stage of the ALU before the preceeding LSB has fully exited out of the last stage of the ALU. This overlap is the "pipelining" that Jeff is so proud of, for it represents nearly 100% utilization of the ALU and is why the internal compromise of having just an 8-bit wide ALU makes little difference externally.

When the LSB of the PC comes out of the ALU, the CPU/RAM is addressed to return it to Reg 7 at the end of MC-2. Likewise, the MSB of the PC is returned to the top of Reg 7 at the end of MC-3. But at TS-3 in MC-3, just before the MSB of the PC makes use of the internal 16-bit bus to get back to Reg 7 at TS-4, the instruction that has been addressed in external memory comes into the CPU and is placed in the instruction register (IR). One very nice feature of the CP-1600 is that, despite its fast 100-nsec clocking, the external memory is given a very generous amount of time to respond. As can be seen in **Fig. 4**, memories with access times as sluggish as 600 nsec could fit into the span allowed for the external memory in MC-2 and MC-3. The CP-1600 user does not have to specify expensive 300-nsec memories with their higher voltage power supplies. He can get by with inexpensive static NMOS memories running off just +5V.

MC-4 is a wasted cycle for the data side of the CP-1600 CPU chip because everything has to stop while waiting for the control side to decode the IR. This takes about four 100-nsec time slots, since about that number of control-ROM stages exist. To be specific, we show the op code for adding CPU/RAM registers Reg 3 and Reg 1 and storing the result back in Reg 1. **Fig. 2** shows this code residing in the IR. By the end of MC-4, the code has "propagated" through the various ROM's on the control side, and the proper signals have been sent back across the "trough" in the middle of the CPU chip to execute the ADDR instruction.

In TS-1 of MC-5, the LSB's of the two operands specified in the instruction—Reg 3 and Reg 1 in the CPU/RAM—are addressed. The codes for the CPU/RAM addresses are literally what you'd expect the CPU/RAM would need, for this microprocessor has a nice straightforward relationship between code and function.

In TS-2 of MC-5, the LSB's of Reg 3 and Reg 1 are simultaneously sent to the ALU to start the addition. From this point on, everything flows naturally, similar to what happened with the LSB and MSB of the Reg 7 in MC-1 and MC-2. The MSB's of Reg 3 and Reg 1 are addressed and started into the ALU in MC-6, just as the LSB result comes out and is returned to the specified results register, Reg 1.

Now note that the final MSB result does not come out of the ALU and get back into Reg 1 until MC-7. Of course, you'll complain: "I thought you said this instruction only took six cycles and 2.4 μsec. This is seven cycles and 2.8 μsec!" So what! At the end of MC-6, the read side of the CPU/RAM is free and ready to send out Reg 7 as PC to fetch the next instruction, and that's all that counts. If you look back to MC-1, you'll see that the previous instruction was likewise finishing up as this instruction was started. (It would only matter if the final result of the computation had to be known in order to determine what PC value should be sent out, as in some branch-type instructions. However, the CP-1600 instructions don't include computations that spill over into the next fetch.)

What does a 16-bit machine give?

It is no accident that the overwhelming majority of minicomputers have settled upon the 16-bit word length. The arguments in favor of 16 bits vs. either shorter 8 or 12-bit lengths, or longer 24 or 32-bit lengths, are very well stated in several articles (**Ref. 5**) that analyze how users should choose minicomputers. In particular, one author in **Ref. 5** who is from a process control company—J. L. Butler of Fisher Controls Co.—details the rationale for settling upon 16-bit words in industrial control computers.

He points out that it is not just a matter of the 16-bit word being best suited for the accuracy of data needed in process control, but that the 16-bit word provides sufficient bits in the machine's instructions to give the user the desirable software options. The lack of instruction-word bits in 8 and 4-bit μP's typically forces them to resort to an unsymmetrical balance between their data and control words. You can see an extreme example of this in early 4-bit machines like the MCS-4 where the control word is eight bits while the data word is four bits, and the address word 12 bits. It is awkward for the instruction words and the data words to share the same hardware, and in fact, in the MCS-4, the two are kept entirely separate and provided with different memories.

This works out fine for small controller applications where the need for data memory doesn't exist anyway, but it becomes expensive for larger systems that must have, say, 4k of RAM. Much of the economy of the SP/GP/DC (stored-program, general-purpose, digital computer) is based upon continuous, repeated utilization of the same circuitry by both data, instructions and addresses, and it is only when the words are the same size

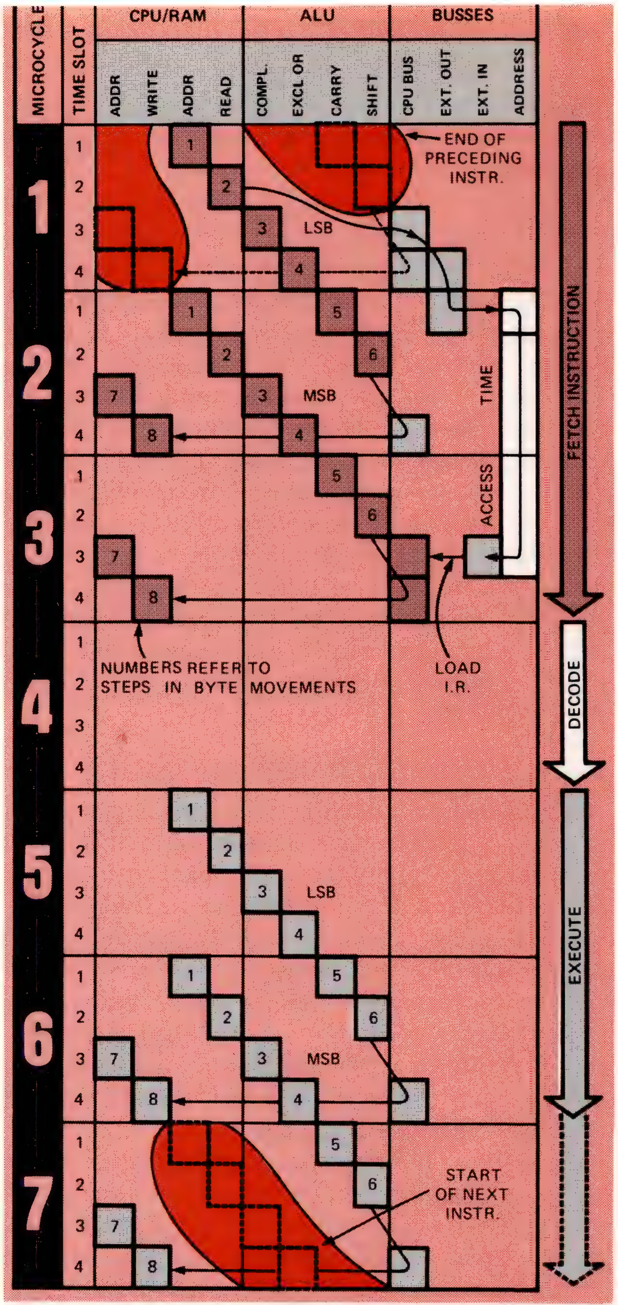


Fig. 4—Musical chairs to a 10-MHz beat, with no bit a loser. A diagram of how 8-bit bvtes are stepped through the CP-1600 ALU in fetching and executing instructions shows the ADDR instruction, which adds two CPU/RAM registers together and stores the result back in one of the registers. Each set of diagonals sloping down to the right represents a halfword byte of the CP-1600's 16-bit registers being addressed and "pipelined" through the four stages of the ALU. Note the high degree of overlapping and how it always keeps the ALU busy.

that this can happen.

As we have mentioned, this first model of the CP-1600 is somewhat of a compromise because there was only enough room on the chip for a 10-bit instruction register. This is a bit awkward, for the CP-1600 must use an odd-sized 10-bit program ROM, and then the instructions can't carry full 16-bit wide literal data (constants supplied as part of instructions). Still, the CP-1600 instruction set shows the value of the extra four bits over the usual 8-bit instructions of 8-bit machines. For example, there is now room not only for the basic 4-bit code, but for two 3-bit addresses for the CPU/RAM registers. Our ADDR instruction could not have been specified by an 8-bit instruction.

Where will it all end?

The shape of "wide-word" microprocessor progress in the next few years becomes clearer as one studies new machines like the CP-1600. While MOS technology is up against limits in speed, it is not yet up against any hard limit in ultimate chip complexity. For the immediate future we can expect to see MOS µP architects like Jeff Stein expend their efforts in imitating the best of large machine architectures that have evolved slowly over the past three decades. Right now, it's obvious that they are gaining on top-of-the-line mini's like the PDP-11. Next it can be assumed they'll tackle medium-scale mainframes, and then maxicomputer mainframes (possibly subdividing the task as Rockwell has done with its DMA chip, which is really sort of a mainframe subsystem).

For example, Jeff plans to start work on a "super" version of the CP-1600 towards the end of 1975 when some finer geometry design rules now in R&D at GI are released for production use. This super machine will have a full 16-bit instruction register (IR). The extra width will allow Jeff to make the CPU/RAM registers as fully general-purpose as those in the PDP-11. The super-16 will have such desirable big-machine features as generalized indexing and hardware multiply and divide. These features will make the µP that much more attractive to users because it will be easier to program. □

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*(*Note: Readers wishing to receive this directory write to: EDN µP Reprint, 221 Columbus Ave., Boston, MA. 02116. The 112-pg. reprint contains Ref. 4 and 13 other EDN features on µP's. Price is $6.95. Check or money order must accompany all requests.)*

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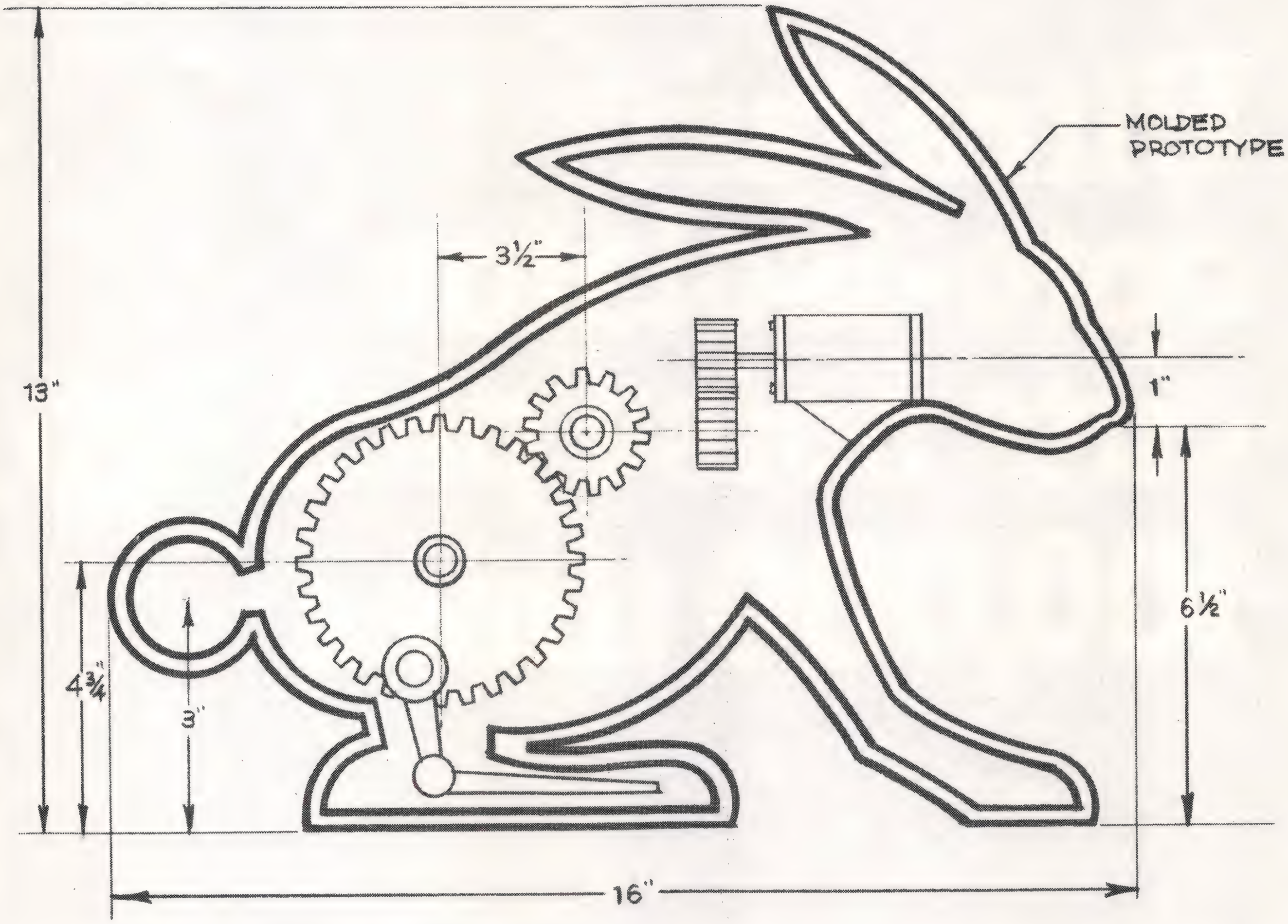

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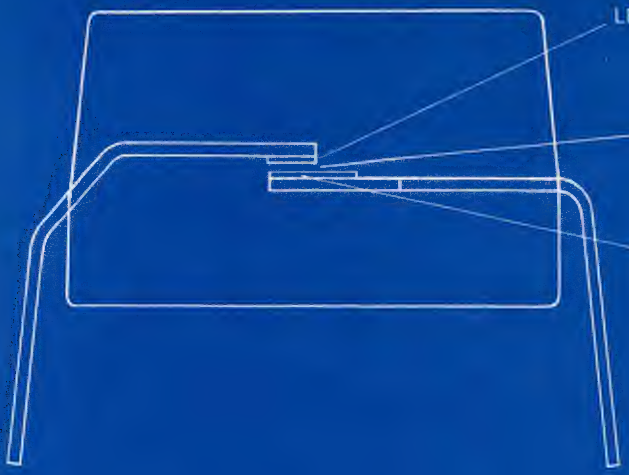

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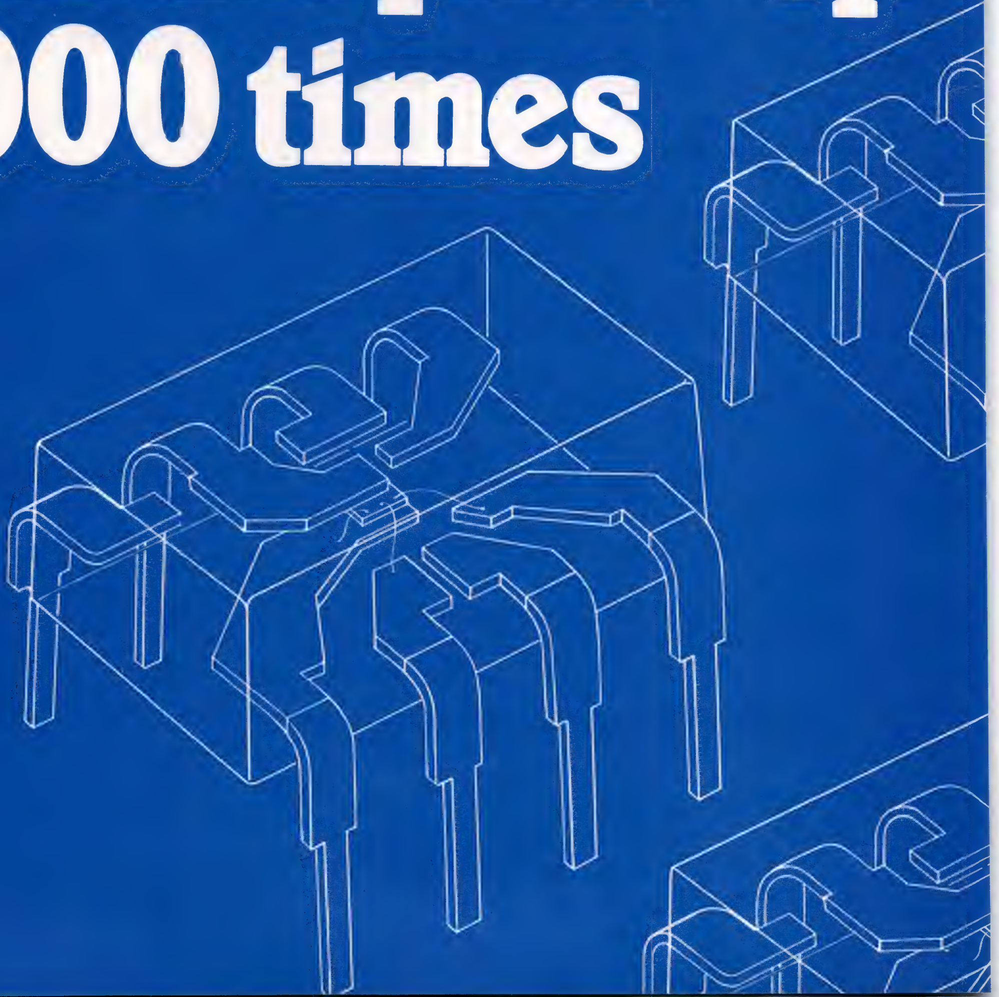

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I²L: Today's versatile vehicle for tomorrow's custom LSI

Integrated injection logic approaches the ideal, combining low cost processing, high packing density, low dissipation and good speed.

Joel Altstein, Associate Editor

From the beginning of its relatively short history, Integrated Injection Logic (I²L) has captured the attention and imagination of semiconductor circuit designers. In ripples, then waves, it has spread rapidly across the industry. Even now, with recessionary pressures choking R & D budgets, I²L projects are going strong. Heads everywhere are beginning to turn towards this promising technology—with good reason, as we shall see.

Any investigation of a semiconductor process invariably reduces to an analysis of basic design goals. Therefore let's apply to I²L the yardsticks by which all technologies are judged:

- economy-cost per bit
- power dissipation per bit
- speed performance
- area per bit
- reliability

and see how the process compares with its peers.

Something old, something new

I²L is a logical extension of a bipolar design technique, a sophisticated subset of TTL. In an atmosphere heated with controversy and favoritism towards logic families and design criteria, it becomes apparent that specific technologies will not make it into LSI. Certain techniques, because of their inability to drive off-chip loads, will not be effective vehicles for logic families. Some, because of their increasing consumption of power at increasing frequencies, will not be used for high-speed memory systems. Each design, then, is destined by its inherent characteristics to occupy a distinct plateau.

I²L's strength lies in LSI use. Its fluid concept will allow processing advantages to be passed on to the customer almost instantaneously. By contrast, existing logic families pay the price of stability; for example, specs for TTL haven't changed for years. Manufacturers place stress on consistency, and optimize processing to give better yields. I²L, however, will be at the other end of the spectrum. Stress will be placed on improving technology. Yields won't be optimized, the technology will.

For the tactical reasons of I²L's birth, we must investigate the design philosophy used in its creation. For the fascination that has caught the designer's eye, we enter the domain of beauty and minimization of the purest sort.

The creation of a cell

The structure of the simple-minded I²L circuit (**Fig. 1**) consists of a lateral pnp whose collector is connected to the base of a multicollector vertical npn. If V_{be} remains constant, current i_b will also be constant and we can represent the structure as shown in **Fig. 2**. Current is injected into the base of the vertical inverted npn transistor.

To build up a circuit, you simply connect one of the collectors of the drive transistor to the base of another lateral transistor. All that is wanted, therefore, is a β of 1, although most β's of I²L transistors are 5-10. One doesn't need exotic techniques to achieve low beta's. However, the vertical npn is unusual—it operates in the inverse mode.

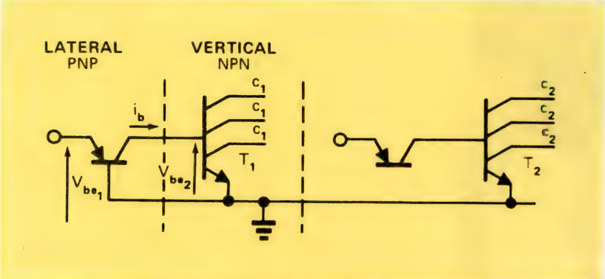


Fig. 1—For proper operation V_{be2} should be smaller than V_{be1} by at least KT/q or 25 mV.

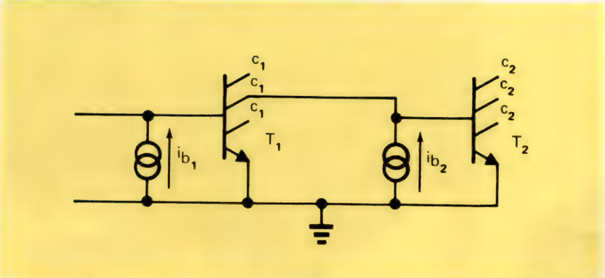
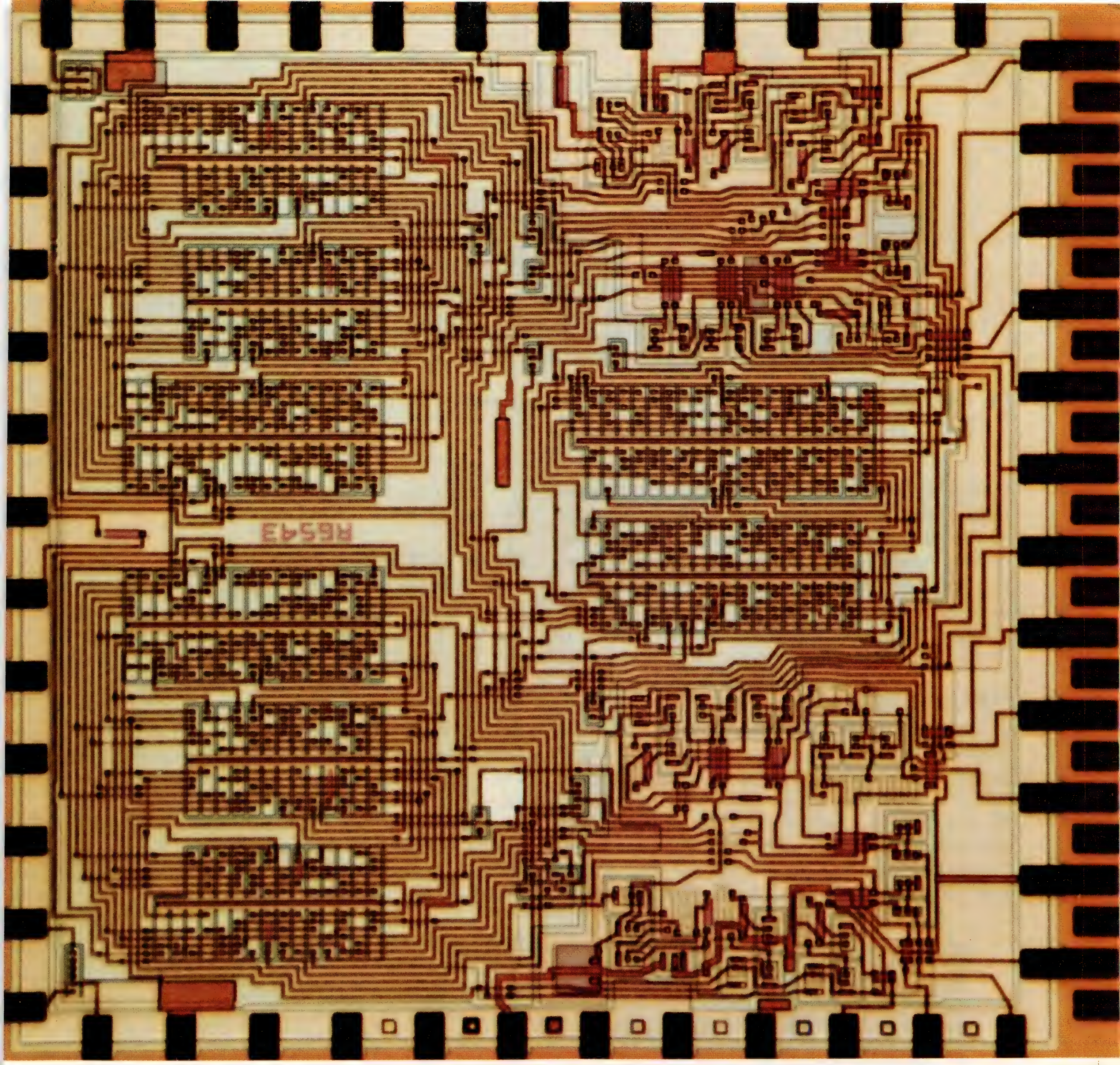


Fig. 2—The basic logic characteristic of this I²L gate is that of an inverter with many separate outputs.



About 75% of this chip area is devoted to I^2L circuitry and interconnection. The remaining area is devoted to TTL interface buffers. The circuit contains 256 equivalent gates and has a total active area of 12,500 sq. mils. *(Courtesy Bell Labs, Allentown, PA)*

There is not a great deal of design and process expertise in building inverse transistors. One must optimize the process to keep inverse β high, while maintaining the process simplicity needed to keep the product cost effective.

What's backwards is inverted

When you build a normal IC device, optimization occurs if you have a relatively light-doped collector, a heavier doped base and a much heavier doped emitter. Diffusion is accomplished from the top surface causing each successive area to become smaller and smaller, quite similar to concentric circles. This method is ideal for collection of the majority carriers. The emitter, on the surface, injects current carriers that traverse across the region to the buried collector.

In the I^2L structure though, the emitter is buried to keep the process simple (**Fig. 3**). This makes sense, since the base of the lateral injector has to be tied to ground and the vertical emitters have to be tied together to make the buried layer common to both. Similarly each vertical collector needs to be isolated; placing them on the surface makes processing even easier.

A contributory, though not decisive, factor in β roll off is that the diffusion process stays the same. You still diffuse from the top surface. This

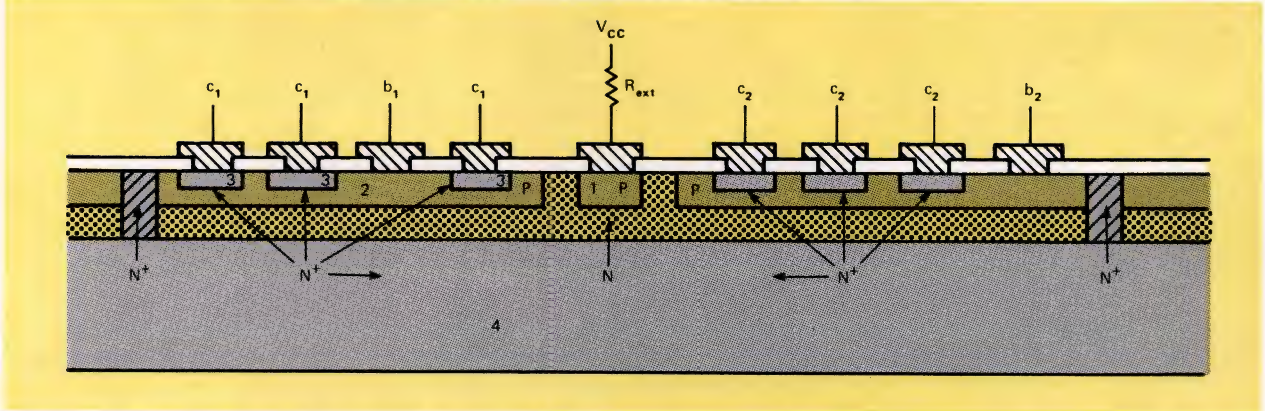


Fig. 3—The P region, labelled 1, is the emitter, while the region labelled 2 is the collector of the lateral pnp transistor. Regions 3, 2 and 4 make up the vertical I^{2}L transistor.

means that the carriers get to heavier and heavier doped areas as they traverse from the I^{2}L emitters to the I^{2}L collectors. No longer are the carriers quickly swept by the potential gradient towards the collector. This process is inefficient. However, each vertical collector only needs a fanout of one. Beta's and, therefore, current collection can be kept at a minimum.

Hail to the chief

Among the various figures of merit that serve as windows to a semiconductor performance, none is more impressive than the speed power product (SPP). All semiconductor technologies can be distilled into one number. This number (or curve) represents the culmination of complex engineering techniques. Few parameters are clear to all, few parameters give pleasure; but this one does.

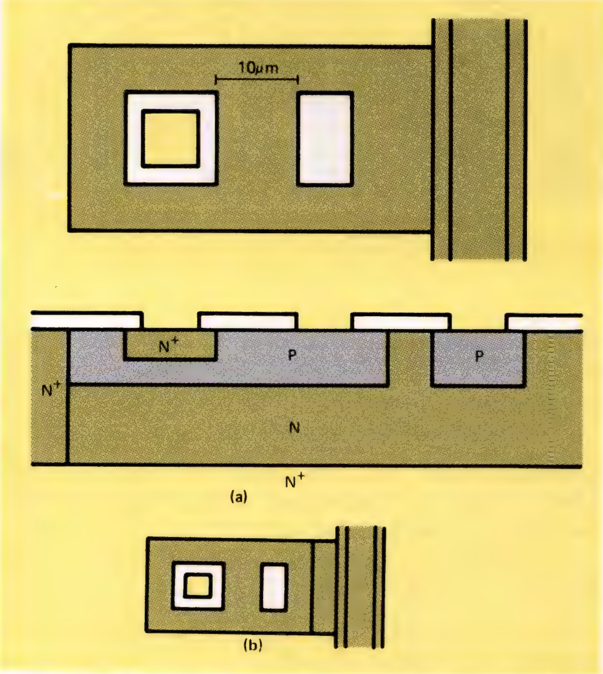


Fig. 4—The layout and cross section are based on minimal dimensions of 10 μm, with diffusion depths not to scale in **a**. In **b**, layout is based on minimal dimensions of 5 μm.

It is technology pure and simple and this is where I^{2}L excels.

Hands across the water

Techniques to increase β and in turn the SPP continue at a fast pace. Experiments to decrease the SPP by decreasing the linear dimensions of the basic gate and keeping diffusion depths constant have been reported.[1] The SPP has been decreased from 1 pJ/gate to 0.25 pJ/gate by decreasing the dimensions of the contact holes from 10 μm to 5 μm and the other dimensions correspondingly (**Fig. 4**). Packing densities of 400 gates/mm^2 have been obtained using this method. Geometric considerations can further decrease the SPP to 0.13 pJ/gate (**Fig. 5**) and, if combined with shallow diffusions, propagation delays of 7 nsec can be achieved.

New geometry, better curves

In the brisk and growing investigation of I^{2}L, further geometric improvements have decreased the SPP to 0.05 pJ. Here the npn transistor is arranged vertically above the injector (**Fig. 6**). Sharing common regions and having lightly doped P-type epitaxial layers, the base contacts can be Schottky-barrier diodes. Now two or more isolated lines can drive the gates. Their inputs will behave like a conventional NAND gate, while still retaining the multioutput of conventional I^{2}L.

Contemporary I^{2}L runs at 15 to 40 nsec/gate, and that's at a 1 pJ SPP. In fact, I^{2}L's SPP is essentially a straight line. The uniqueness of the circuitry is that you can set the operation of the device at any place along the curve without changing components in the circuit. By merely adjusting one external resistor, you can determine chip current and, hence, the operating speed. You can have, in certain custom applications, entire circuit functions working at predetermined speeds. If you wish to minimize off-chip drive, you can exit the chip at TTL levels. This is accomplished by placing TTL buffers right on the chip.

In bipolar technologies, once the gate resistor values are set, you are locked into a specific power dissipation. TTL comes in three to four speed power ranges and the basic designs differ for each family. Essentially, the resistor's values are completely different for each family. In Schottky TTL, to achieve low-power dissipation, resistor values are four to five times higher than in standard TTL. I²L avoids all this. The flexibility of not having load resistors opens up completely new areas of operation.

Increasing packing density

Shared semiconductor regions quite naturally increase packing densities. In addition, the inverted structure of the planar vertical switching transistor almost automatically achieves further density improvement. Placing the multicollectors of the output transistors on the surface immediately achieves isolation. Finally, layout and geometry rules (when firmly established) will have an additional salutory effect on packing densities.

For almost identical reasons that packing densities increase, β degradation occurs. Problems arise because semiconductor regions of the same doping densities act both as the emitter of one transistor and the base of another. As mentioned earlier, β's suffer because of the inverse structure of the switching transistor. These problems can be solved with increased N+ isolation diffusions. Increased isolation, though, adds to the total fabrication costs, while the better packing densities it permits mean more effective use of silicon real estate. Thus, you have a trade off.

How does it compare?

Although bulk CMOS has the potential and, in some cases, has achieved LSI, most available CMOS performs TTL functions. CMOS seems to be limited to small-scale integration (SSI) and medium-scale integration (MSI). As I²L is to T²L, so SOS-CMOS is to bulk CMOS.

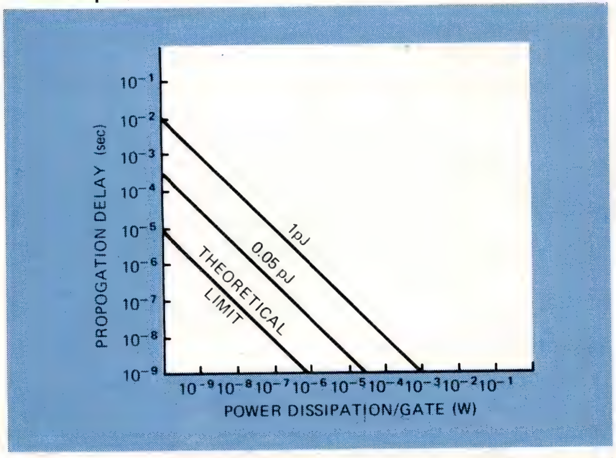


Fig. 5—Geometric considerations determine the shape of these curves. By applying a geometry in which current is injected into the npn transistor from three sides, instead of one, further reduction in the SPP is anticipated.

SOS-CMOS allows you to retain the permissiveness of CMOS while attaining a 2:1 density and 10:1 power dissipation and speed improvement over CMOS. SOS-CMOS noise immunity and liberal power supply variations are well known. SOS is, in fact, the ultimate MOS technology. Its only limiting factor in speed is the inherent gate capacitance, all other capacitances are negligible.

With the perfection of ion implantation and self-aligned silicon gates, 10V SOS can operate at 1 to 2 nsec/gate. In terms of any parameter you choose, SOS beats bulk CMOS except for cost. Presently the price of a sapphire substrate is six to seven times greater than bulk CMOS (for a 2-1/4-in.wafer). Processing of SOS-CMOS is one-third simpler than bulk, requiring only six masks. Certainly in conditions where noise and/or radiation are factors, SOS would prove to be the better avenue to take.

SOS-CMOS products are beginning to make a market impression with the release of RCA's oscillator/ripple counter circuit. The unit, primarily intended for time-keeping applications, where low power (single-cell 1.5V silver-oxide battery) and high speed are required, draws 9 μA at 4 MHz. The circuit consists of an input amplifier for use in a crystal oscillator, followed by 23 stages of binary division. Soon to be released is a 1k, 16-pin RAM with access and cycle times of 120 nsec with 4k static RAM's to follow. High-speed divide-by-N counters for portable battery-operated communication equipment and μP's represent likely candidates for the next generation of SOS-CMOS products.

SOS has been a fixed target, beginning to show some movement only in the past 18 months. New entries into the LSI field might not want to make the major financial commitment SOS requires. They might, with less levels of investment, be able to attain LSI goals with I²L. Indeed the initial

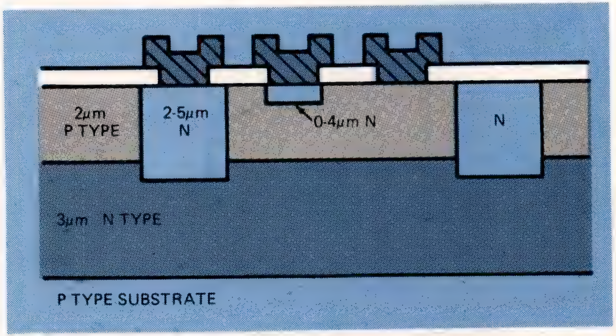


Fig. 6—Substrate-fed logic—the npn transistor is arranged vertically above the injector. The substrate is the emitter of the pnp transistor whose base and collector are epitaxial layers, acting as emitter and base while the collectors are diffused N regions.

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I^2L has an important extra advantage over SOS technology at the high-frequency end of the operating spectrum. At these frequencies, the power supplied to the I^2L chip is independent of what's going on in the chip.

Friend of ECL

One of the more striking comparisons you can make with I^2L is its similarity to emitter-coupled logic (ECL). Process technology similar to TTL has been used to fabricate ECL RAM cells. Both technologies attain desired operation through current stirring. The ECL memory cell requires a constant current supply, which is shared by a number of cells. Current is directed to differential pairs. The current in an I^2L circuit is constant, similar to ECL. On the other hand, TTL, like MOS, is a voltage form of logic; current depends on the state of each element and varies dramatically.

What's in the future?

MOS faces a serious challenger in I^2L. The initial round in the LSI area has been awarded to MOS/FET technology, but the jury is still out.

Standard I^2L today can be operated in the area bounded by TTL and p-channel MOS (10-100 nsec). N-channel operation lies somewhere in the middle of this range and that's where I^2L can compete very effectively. In systems that are not power limited, speed becomes the essential parameter of interest. Here, through geometric techniques that will minimize area and maximize speed, I^2L will become a viable alternative in the LSI arsenal. ☐

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Acknowledgement

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And to those who wish to remain forever nameless—thanks!

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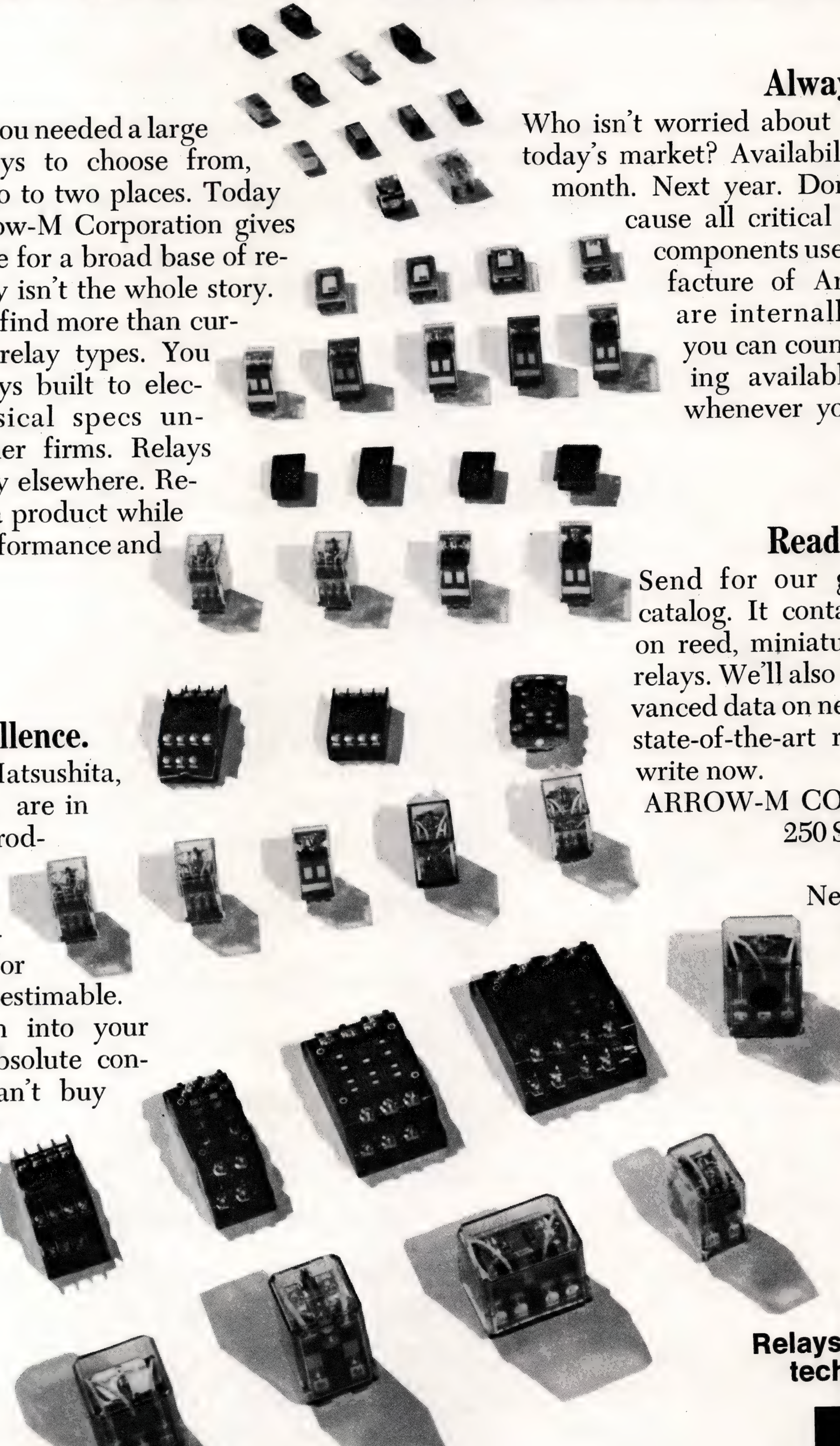

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Film	6	10	▼
Mica	13	16	▼
Paper	7	11	▼
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Coaxial	7	12	=
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high-density	10	14	▼
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	LEADTIME IN WEEKS		
	MIN.	MAX.	TREND
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Wirewound	3	8	▼
RESISTORS, VARIABLE			
Nonwirewound			
nonprecision	3	7	=
precision	5	10	▲
Trimmers	4	10	▲
Wirewound			
nonprecision	3	8	=
precision	4	8	=
trimmers	3	8	=
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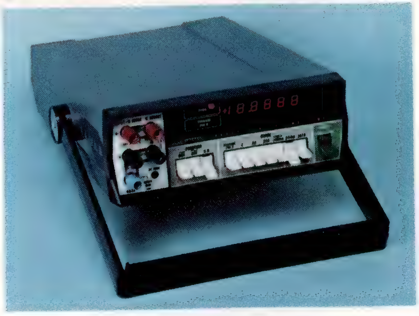

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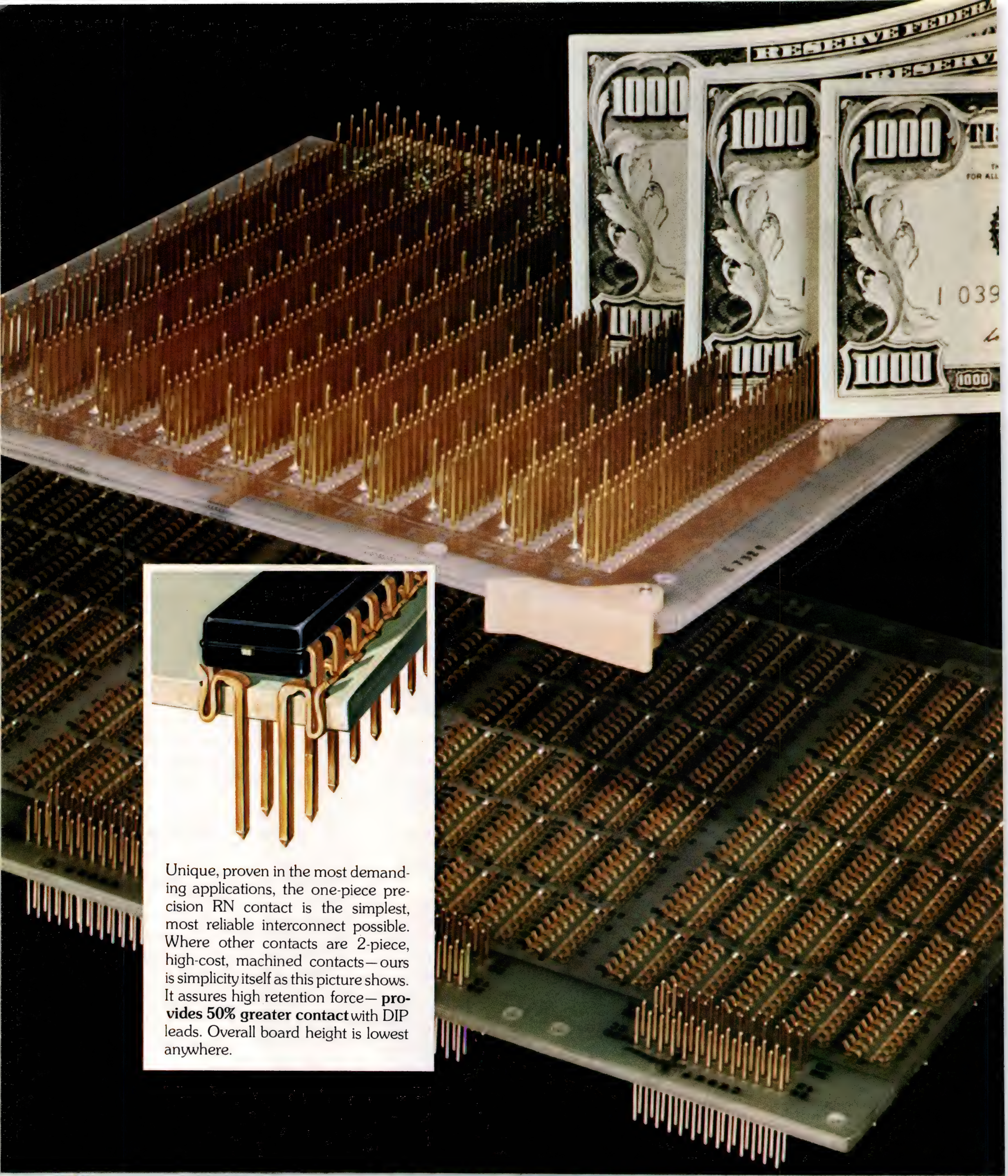

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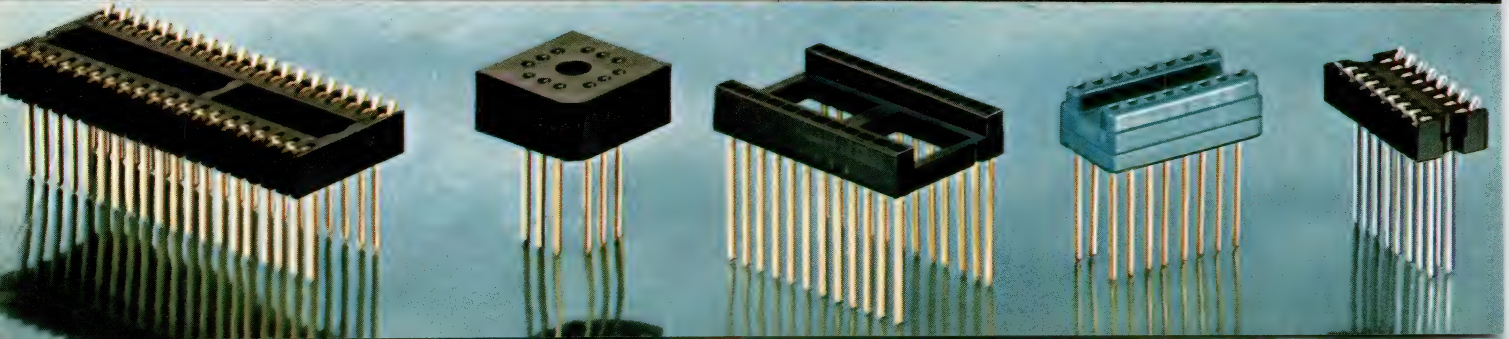

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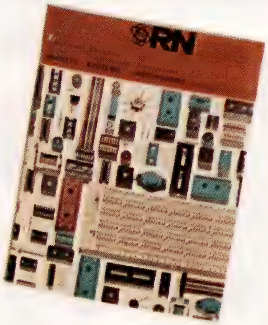

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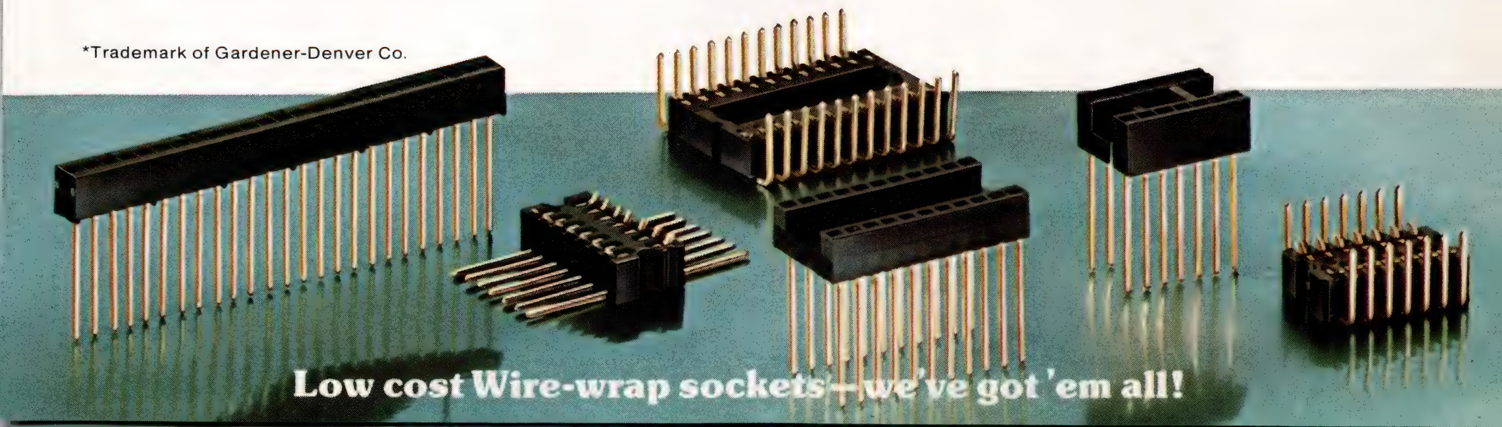

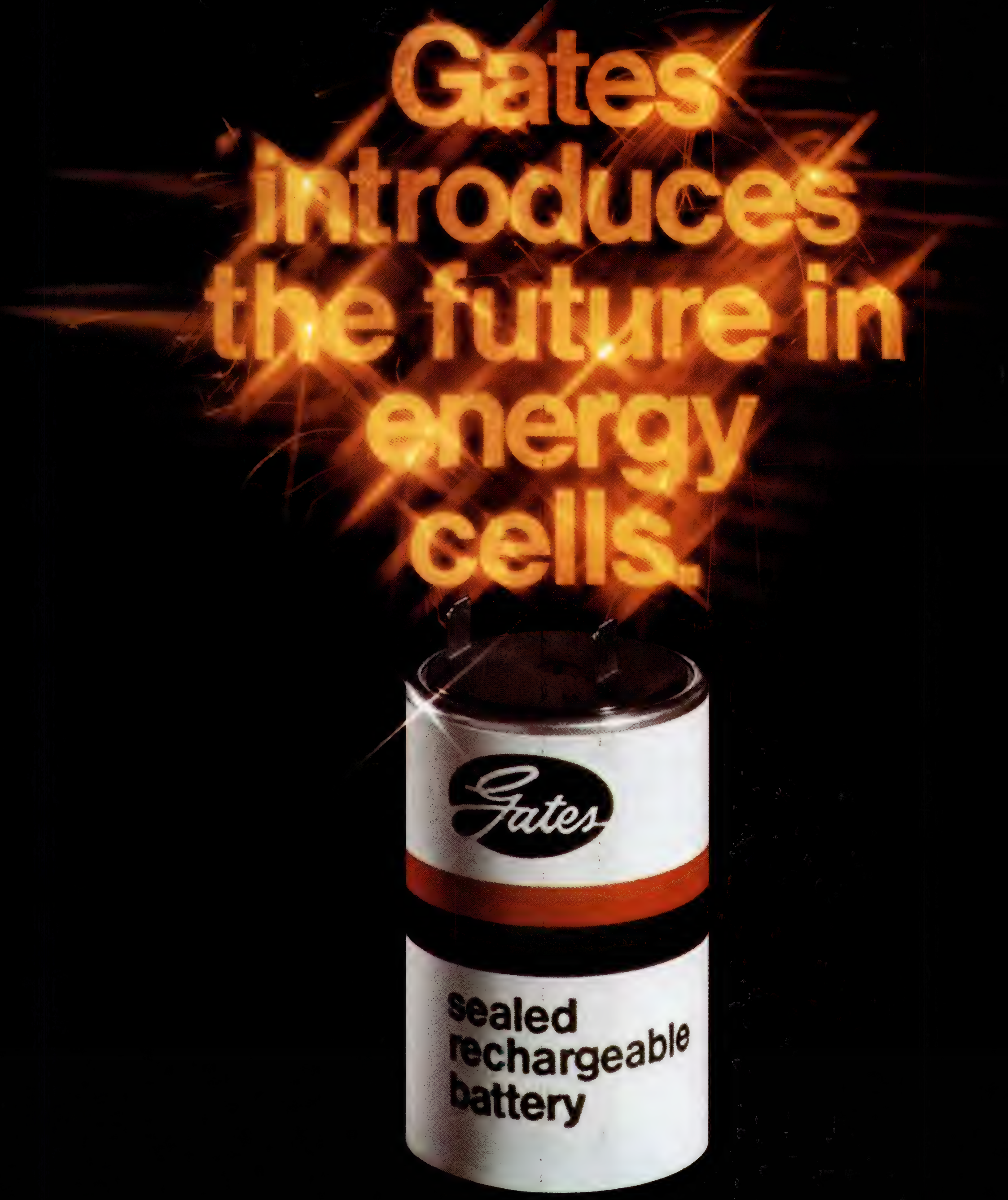
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Able to leap µP's in a single bound—the ABDAT processor

Using just a handful of OTS logic chips, ABDAT is cheaper, better and faster than anything you can buy in 1975—even a 1974 model.

Arnis G. Butulis and **Dan Torbeck**, Monarch Marking Systems

The area of micro-computing has been overstudied, overwritten, overemulated and oversimulated. Logic designers have become saturated with buzz words of the micro world. But buzz words do not build systems. Thorough knowledge does, and this knowledge has been hard to come by. For a long time µP's have not matched the price and performance of processors constructed from off-the-shelf (OTS) random logic. But rather than shed light on the art of micro-computing, the industry has been too busy telling the world why a particular processor is so much better than another.

In the beginning

In 1951, Wilkes presented the basic model of micro-programming. Liberally translated, the model was a read-only memory which outputted its own next address plus data (**Fig. 1**).

This memory would start at input address ZERO (binary 000). For an input of ZERO, it would output the address ONE (binary 001) plus a data word, say 01010, on the five data lines. Cycling would continue until the input address reached SEVEN (binary 111). The output address would then become ZERO and the cycle would start over again.

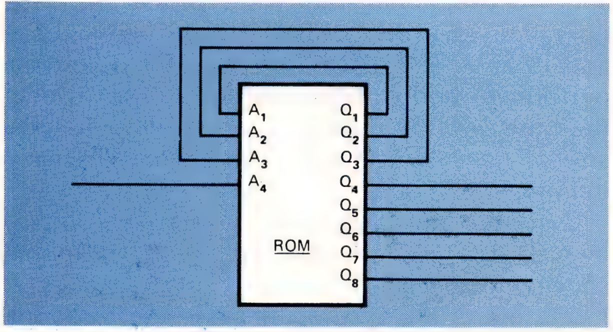


Fig. 1—A ROM, connected as shown, is the simplest type of micro-programming model.

STEP NO.	INPUT ADDRESS	OUTPUT ADDRESS	DATA OUTPUT	
0	0000	001	01010	
1	0001	010	01001	
2	0010	011	01111	
3	0011	100	01111	
4	0100	101	01111	
5	0101	110	01111	
6	0110	111	00011	
7	0111	000	00011	
8	0000	001	01010	
9	0001	010	01001	
10	1010	011	11100	JUMP
11	1011	100	11100	
12	1100	101	11100	
13	1101	110	10000	
14	0110	111	00011	
15	0111	000	00011	
16	0000	001	01010	
17	0001	010	01001	

Table 1—SIMPLE JUMP INSTRUCTION

One could spend several weeks playing with this model because the logic design possibilities are truly inexhaustible. For example, the ROM in **Fig. 1** has one additional input brought to the outside world. **Table 1** shows the ROM map when this fourth input line is toggled.

For buzz-word enthusiasts, **Table 1** describes the basic operation of a controller. The controller does something in a predetermined manner until it is told (input line A_4) to do something else. It can control itself or other devices, such as registers, in a computer or µP.

The second concept is that of computation. To perform a computation (any computation) one needs only an adder/subtractor and two registers where numbers to be operated on reside (**Fig. 2**).

It may come as a shock to micro-sophisticates

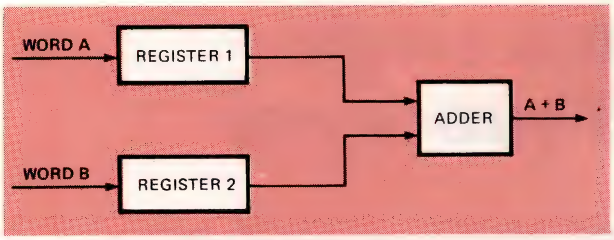


Fig. 2—A basic parallel adder requires only two extra storage registers to enter data into the arithmetic unit.

(pun intended), but the two previous ideas (i.e., microprogramming and a simple adder/subtractor with some storage registers) constitute a full blown μP.

The outcry of charlatan may be temporarily entertained. Indeed, an adder cannot perform a logical AND instruction, nor can it perform a JPZ or JPP (jump on zero or jump on positive) instruction. Also, it can't perform masking nor can it perform two dozen other instructions.

Do we really need an instruction set?

Let's examine for a moment the usefulness of instructions and higher level languages. Today's vogue is to use micro's to copy mini's. This results in a residue of assembly languages, compilers, cross-assemblies, Fortran, etc. Again we must ask: Are these really necessary?

It has been proven time and again that the best language in terms of hardware economics is machine language.

Fortran programmers are limited by the clever individual who wrote the assembler. On the other hand, the machine language programmer is limited only by his imagination and, sometimes, the limitations of the machine. One reason for the unpopularity of machine language is that it takes longer to write a machine-language program than to write an equivalent one in PL/1 or Fortran. This is true for very large and medium-sized systems, but not for small systems, and it is absolutely false for μP's.

Massive mainframe vs. midget micro

The confusion factor is the following: Big systems, such as the IBM 360's and CDC 6400's, are fixed machines (logic blocks) with continuously changing programs. Witness the large data processing departments accompanying each machine.

Contrast this with microprocessors. A μP is a continuously changing logic block with a program determined and fixed by the equipment of which it is a part. Witness the large engineering departments accompanying their use.

Using a large-scale, single-program computer for monitoring a traffic intersection would be just as ridiculous as using a high-level language on a μP. Even though it could be done, the spectrum of economics is obviously reversed.

The point: If massive, continuously changing programs are of interest, a large computer with highest level languages is in order. If a few short programs are of interest, a minicomputer with its assembly language will do fine. However, if a single program (any multiple unit hardware application) is of interest, machine language is by far the most economical way to go.

To be powerful, a processor does not need a high level language or even a formal instruction set. Conversely, it can have a set of instructions up to 2^{16} or 2^{24}, or even more.

Anything you can do I can do better

Fig. 3 illustrates a simple parallel bus with one control device (microprogrammed ROM) and X, Y, Z, etc. auxiliary devices (such as adders, RAM's, shift registers, temporary registers, FIFO's, etc.) connected to it. The control dictates which device is to talk; i.e., output onto the bus. Simultaneously it dictates which device(s) should be listening.

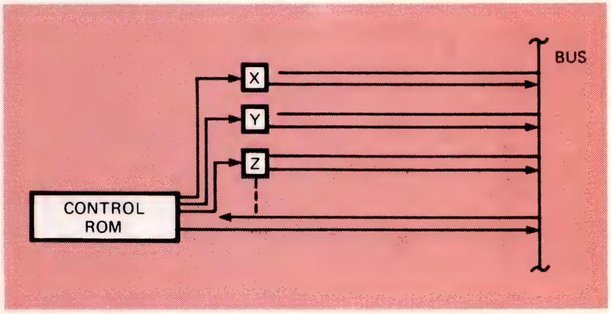


Fig. 3—Parallel bus architecture allows performance of many simultaneous operations. Combine this with a microprogrammed ROM and complex instructions are possible.

Since any or all devices can accept information simultaneously, bizarre instructions such as increment program counter, increment RAM address register, multiply bus contents by two, temporarily store bus contents and output bus contents, are possible—all in one 0.4-μsec machine cycle, and with only one adder. With two adders, a simultaneous A + B and A − C operation can be performed, and with three adders an A × 2 and A + B and A − C can be performed, and with four adders..., and five.... Both the system's expansion possibilities and the size of the instruction set can become virtually infinite.

Using the above concepts, a processor implemented in OTS TTL, would have the specifications shown in **Table 2**.

It is interesting to compare these specifications with those of any available μP; it's even more interesting to compare architectures. Such comparisons show that μP chips are no match for off-the-shelf random logic.

Random logic in the micro-programmed mode offers the logic designer an infinite menu. Microprocessors attempt to put the same designer into the straightjacket of a fixed and very rigid instruction set. This set is then tied to some assembler that was dreamed up by, hopefully, a very clever individual.

SINGLE VOLTAGE	+5 Vdc
FULLY STATIC	0 Hz TO 2.5 MHz
CYCLE TIME	0.4μSEC
SINGLE CLOCK	10 MHz
ARITHMETIC UNITS	1 (EXPANDABLE TO N)
NUMBER OF INSTRUCTIONS	2^{16} (EXPANDABLE TO N)
WORD LENGTH	16 BITS (EXPANDABLE TO N)
WORKING REGISTERS	3 (EXPANDABLE TO N)
BOOTSTRAP START-UP	
FULLY MICRO-PROGRAMMED TIME BASE GENERATOR	
SIMULTANEOUS INSTRUCTION EXECUTION	
OFF-THE-SHELF AVAILABILITY (5 ROMS, 1 RAM, 1 ADDER, ETC.) $130	
POWER SUPPLY	+5 Vdc 2.5A (NOT INCLUDED)

Table 2—OTS PROCESSOR SPECIFICATIONS

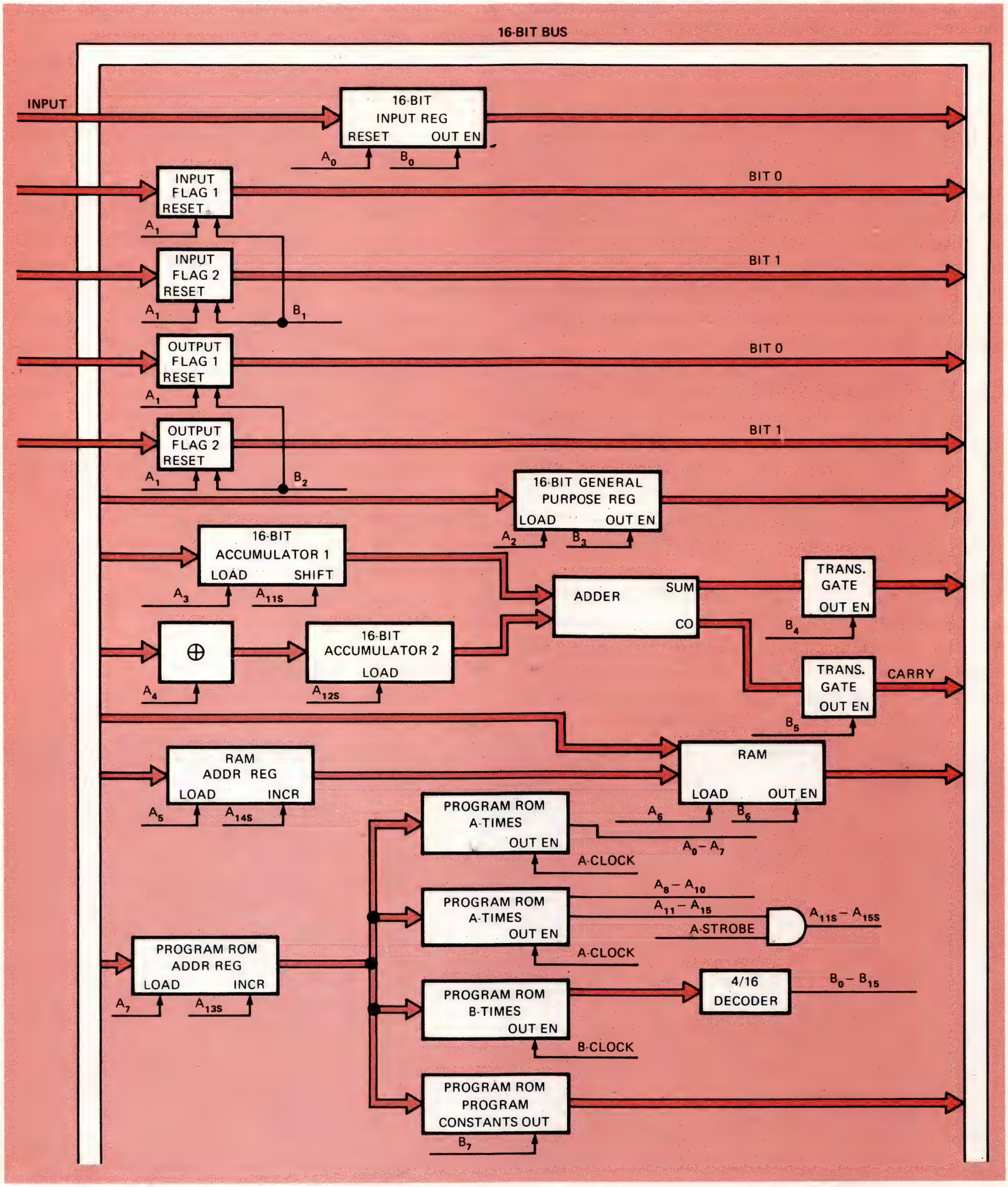


Fig. 4—And now, the ABDAT processor. Architecture for this minimum 16-bit processor combines **Figs. 1, 2** and **3** with the specs in **Table 2**.

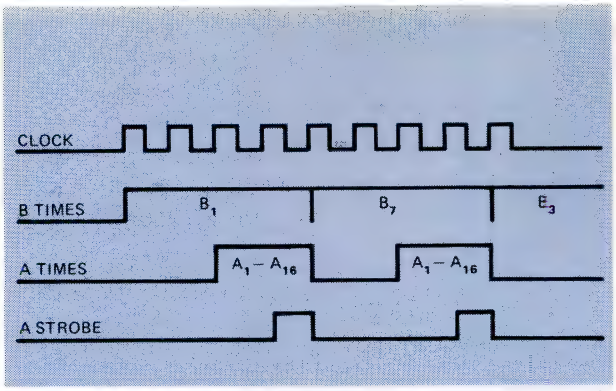


Fig. 5—Programming of the ABDAT processor is done through time-base control lines. Program ROM's determine which time intervals are on, and the clock determines when they are on.

Proof of the pudding lies in the following deed. An 8-bit processor was constructed from standard TTL off-the-shelf parts to perform a rather sophisticated optical data acquisition and processing operation. With 20% less IC's, it performed the function twice as fast as a CMOS hard-wired version. Curiously, a 16-bit machine can do it with 30% less IC's at three times the speed, because of elimination of double precision arithmetic operations on the basic 12-bit data word.

Put your money where your mouth is

Fig. 4 shows the architecture of a typical minimum 16-bit machine. Note that this processor does not contain an arithmetic logic unit (ALU); it contains only an adder. Moreover, it has only three timing intervals: B times, A times and A strobe times. The timing relationship is shown in **Fig. 5**.

During any sequential B time, the addressed device outputs onto the bus. During any parallel A times, bus data can be entered into any or all registers addressed by an A time. During A strobe times, such functions as shift are performed with an "A" time acting as a shift enable.

A micro-programmed ROM with a 1k×4 organization generates B times. A 4/16 decoder decodes the 4-bit output word, enabling 16 different output devices to be addressed. The 16 A times are generated through two micro-programmed 1k×8 organized ROM's. They operate in juxtaposition to output a 16-bit word where each bit addresses a dedicated input device. For example, bit two (A_2), if HIGH, always strobes bus information into the general-purpose register. The input to all three ROM's comes from a single ROM address register with 8, 9, 10 or more bits.

Four typical operations are presented in **Fig. 6**, illustrating the operation of this architecture. First is a simple addition with both numbers input from outside the system. They could just as easily come from the program constant ROM or have been held in the general-purpose register (GPR).

An unconditional jump, the easiest instruction to execute, requires only one program step. Just place the program constant in the ROM address register.

It takes only four instructions (1.6 μsec) to multiply the contents of the input register by five and store the result in RAM location 15. Compare this to existing μP's that take two to three instructions to just double a number.

Shown last, but not least, is the conditional jump. The jump depends on the total input flag count. If neither flag is set (both zero) the program will loop between steps 101 and 103.

Given the power shown above, an imaginative designer, and possibly some parallel processing, there is practically no limit to the capabilities of this type of processor.

Anyone can program it

By now it should be obvious that such a machine does have instructions but does not

PROGRAM STATE NO.	INPUT REGISTER	ACC 1	ACC 2	ADDER	FLAG 2	FLAG 1	RAM ADDRESS REGISTER	PROGRAM CONSTANT	ROM ADDRESS REGISTER	A TIMES	B TIMES	EXPLANATION	OPERATION
1	47								2	0, 13S		LD INPUT REG	ADDITION
2	47	47							3	3, 13S	0	LD INPUT REG INTO ACC1	
3	16	47							4	0, 13S		LD INPUT REG	
4	16	47	16	63					5	12S, 13S	0	LD INPUT REG INTO ACC2	
5	16							96	96	7	7	LD PROGRAM CONSTANT INTO ROM ADDR REG	UNCONDITIONAL JUMP
96	16	16	16	32					97	3,12S,13S	0	LD INPUT REGISTER INTO ACC1 AND ACC2	MULTIPLY BY 5 THEN STORE
97	16	32	16	48					98	3, 13S	4	LD SUM INTO ACC1	
98	16	64	16	80			15	15	99	5, 11S, 13S	7	SHIFT ACC1 ONCE AND LD 15 INTO ADDR REG	
99	16	64	16	80			15		100	6, 13S	4	LD SUM INTO RAM LOCATION 15	
100		103			0 OR 1	0 OR 1		103	101	3, 13S	7	LD PROGRAM CONSTANT INTO ACC1	CONDITIONAL JUMP
101		103	0,1,2 OR 3	103–106	0 OR 1	0 OR 1			102	12S, 13S	1	LD FLAGS INTO ACC 2	
102		103	0,1,2 OR 3	103-106	0 OR 1	0 OR 1			103-106	7	4	LD SUM INTO ROM ADDR REG	
103		103	0	103	0	0		101	101	7	7	LD PROGRAM CONSTANT INTO ROM ADDR REG	
104		103	1	104	0	1		195	195	7	7	LD PROGRAM CONSTANT INTO ROM ADDR REG	
105		103	2	105	1	0		200	200	7	7	LD PROGRAM CONSTANT INTO ROM ADDR REG	
106		103	3	106	1	1		210	210	7	7	LD PROGRAM CONSTANT INTO ROM ADDR REG	

Fig. 6—Many operations are possible with the ABDAT processor. The four presented here are typical illustrations of machine power available.

have a specific instruction set. Instead the designer tailors the instructions to fit hardware needs. Absence of an instruction set enables anyone (an arithmetically-inclined engineer will do) to start programming the device immediately without extensive instruction set memorization.

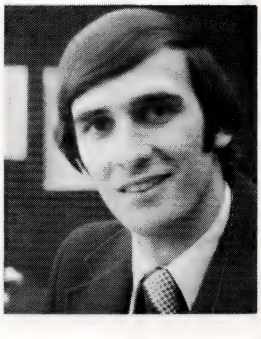
A note about manufacturing and service is in order. The truth table for the register contents and the microprogram also serves as a step-by-step debug map. Since the machine operates at dc, it can be single stepped until the incongruous program step is found, thereby pointing to the faulty device. Indoctrination of an entire manufacturing operation into assembly language, μP, etc. is unnecessary; anyone familiar with logic can, without much training, debug an ABDAT processor.

To be sure, present day μP applications replace minicomputer functions on a onesy-twosy basis. They are not, however, price or speed competitive with microprogrammed random logic when it comes to volume production systems. Face it, this is really what concerns most logic designers.

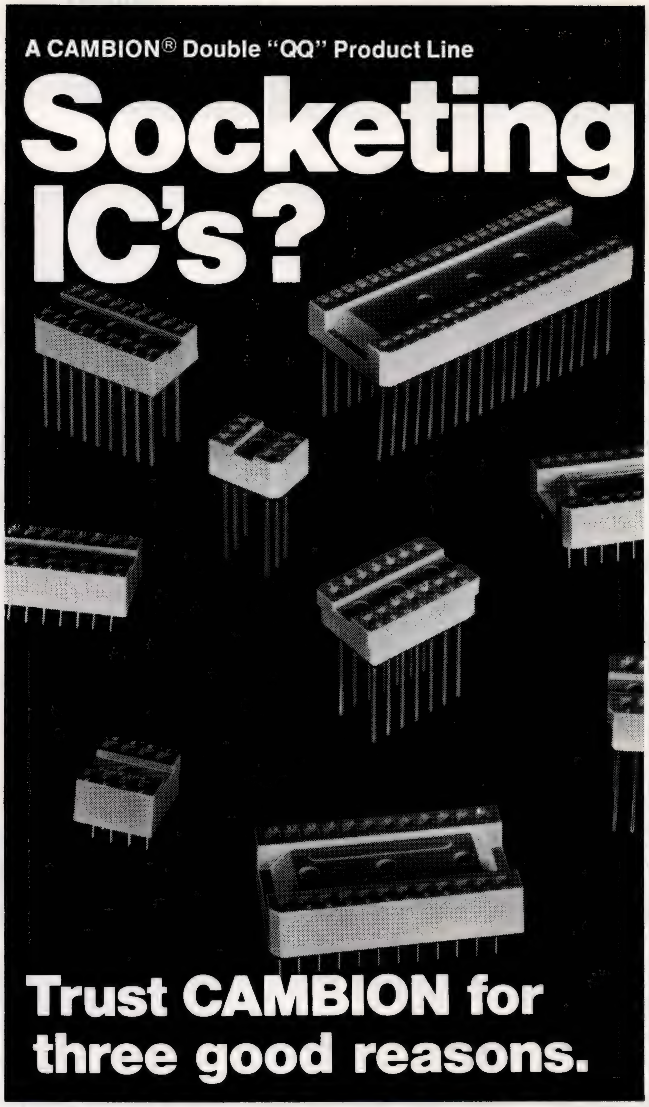
Next time you have an application for a μP, think for a moment about that unit that sells for $300 to $1000. It probably requires a hardware simulator, a software IBM 360 or timeshare emulator, a teletype, 3″ thick documentation and operating manuals. Then think for a moment about this article and the $130 unit we have described. ☐

Authors' biographies

Arnis G. Butulis is Engineering Manager of optical code scanning systems for Monarch Marking Systems, Inc., of Dayton, OH. He received his BSEE from Oregon State University. A member of IEEE, Arnis has one patent pending. Outside interests include golf and skiing.



Dan Torbeck is a Design Engineer with Monarch Marking Systems, Inc. His present work includes design and development of firmware and microprocessing support for bar code scanners. Dan received his BSEE from the Univ of Cincinnati.



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Solve phase stability problem in AM receivers with PLL techniques

The phase stability problem has long retarded widespread adoption of synchronous detection. IC PLL's make this problem disappear.

Thomas Mollinga, Technical College, Zwolle, the Netherlands

Before FM became a fashionable communications system, AM double-sideband (DSB) transmission was the only mode of commercial broadcasting. Although it suffers in many ways when compared to FM, AM easily wins the contest when it comes to reception range. Unfortunately, this very quality has also become a source of problems.

In Europe, the most extensively used band in commercial AM broadcasting is the medium-wave band (500-1600 kHz). However, its popularity has resulted in a rather chaotic situation, for during the past decade, more and more stations have penetrated this band. Although frequency allocation and bandwidth limitation (9 kHz) have been set by international agreement, compliance is sadly lacking. Many of the new stations transmit up to frequencies in excess of 10 kHz, and often exceed the permissable power. This is quite noticeable when tuning across the band, because in addition to some legal program material, you hear a liberal dose of repulsive sounds.

A problem of economics

In essence, AM broadcasting consists of: DSB transmission with maximum modulation index of 30%; conversion to an IF frequency, usually 455 kHz; and recovery of the audio by envelope detection. This recovery method prevails because it is simple to implement technically, and attractive for mass production of the superheterodyne receivers. Economics aside, however, the system has many disadvantages.

Most stations transmit with a modulation index of less than the allowable 30%. Since both sidebands contain the same information, half of the available spectrum space is wasted. Additionally, random differences in amplitude and phase of the two sidebands result in selective fading.

In conversion to an IF, image responses are generated. In addition, the IF bandpass filters determine the receiver selectivity.

Finally, due to diode characteristics, envelope detection results in distortion at low-signal levels as well as a threshold effect.

Technically, DSB transmission can be changed to single-sideband suppressed carrier (SSBSC) transmission without major problems. Many of the disadvantages mentioned above would be eliminated. The actual problem, however, involves cost and compatibility.

On the receiving end, reception quality can be improved by using synchronous rather than envelope detection. Although the synchronous detection method has been known for many years, technical problems concerning phase stability have prohibited its adoption. However, advances in phase-locking techniques and the availability of integrated phase-locked loops present the long-sought answer to the stability problem.

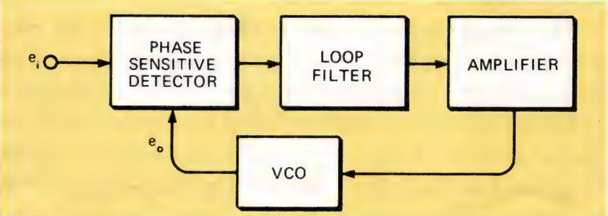


Fig. 1—In the basic PLL, the output voltage of the phase-sensitive detector controls the VCO output frequency.

The PLL has a lot to offer

A block diagram of a basic phase-locked loop (PLL) is shown in **Fig. 1**. Signal input and the output signal of a voltage-controlled oscillator (VCO) are multiplied in a phase-sensitive detector or multiplier (PSD). The PSD produces a voltage proportional to the phase difference between e_i and e_o. After filtering out high frequency components, and amplifying the filtered signal, the voltage controls the frequency of the VCO.

Assume that the VCO is operating at its free-running frequency. If the frequency of e_i comes sufficiently close to that of the VCO, the system will lock and the VCO suddenly synchronizes to the frequency of the incoming signal. Thus, lock occurs if the input frequency falls within a certain frequency range centered around

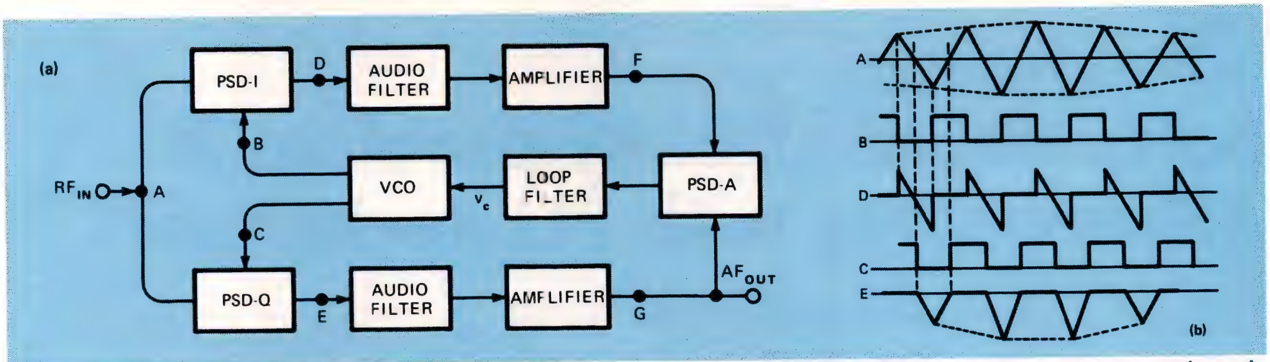


Fig. 2—Because of the phase quadrature of the multiplying signals from the VCO, the basic receiver requires two channels.

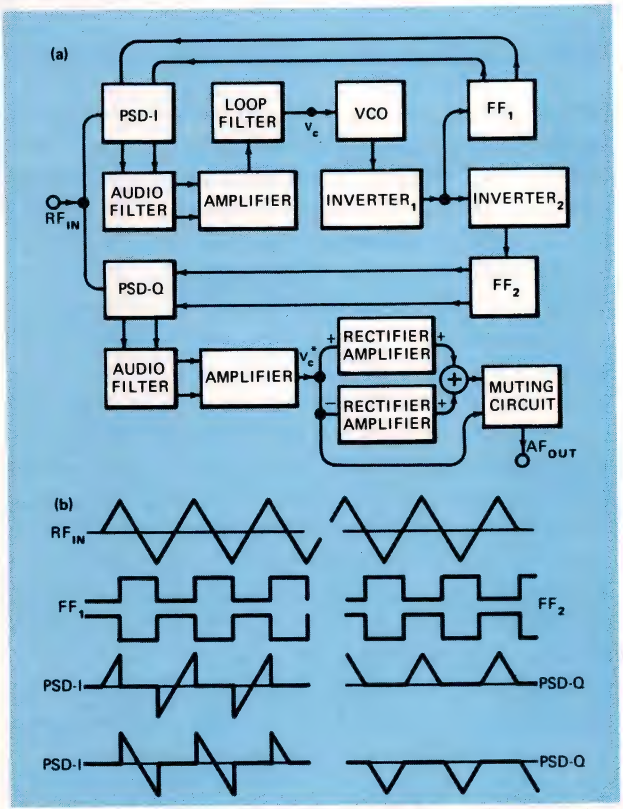


Fig. 3—Digital techniques solve the problem of maintaining phase quadrature at all frequencies.

the free-running VCO frequency. This range is called the PLL's capture range. In terms of broadcast receivers, it's equivalent to selectivity. Once locked, the VCO will track the input frequency over a certain range, called the lock range.

A phase-locked AM receiver provides the following features:

- no image responses, since the IF frequency is 0 Hz,
- selectivity that is determined by the capture range of the PLL, which in turn is set by the time constant of the low-pass loop filter,
- operation hardly affected by selective fading
- RF-to-audio conversion accomplished at very low-signal levels, so that overall receiver gain is obtained mainly at audio frequencies,
- no threshold effect,
- no inductances (apart from preselection circuits),
- signal-to-noise ratio that is preserved at low-signal levels.

A choice of solutions

Although a number of variations of PLL-AM receivers exist, two basic configurations can be set up. One configuration, shown in **Fig. 2**, consists of two channels. An in-phase channel (I-channel) and a quadrature channel (Q-channel) are necessary because of the phase quadrature of the multiplying signals from the VCO. When the VCO is correctly tuned to the RF input, the waveforms at D and E will be as shown in **Fig. 2b**. Audio filters following the PSD's remove all HF components, and pass only audio information.

Both audio signals are multiplied in a third detector, PSD-A. At correct tuning, this detector produces the zero control voltage required to lock the VCO to the incoming signal.

If a small phase error now arises in the VCO, the signal at G decreases somewhat. At the same time, a small audio signal develops at F. Depending on the sign of the phase error, this signal will either be in phase or in phase opposition to the signal at G. As a result, control voltage v_c is either positive or negative. Thus, the VCO is pulled in the proper direction to restore correct tuning.

This circuit's operation is independent of the carrier and is based on sidebands only. By omitting PSD-A, a slightly simplified configuration results. The simplified version is, in fact, the one used in our experimental receiver circuit.

Developing the receiver

The experimental circuit (**Fig. 3**) requires two VCO signals, which are in phase quadrature at all frequencies. Digital techniques offer an elegant solution to this problem. The VCO oscillates at twice the RF frequency, and its output signal triggers two flip-flops. As the flip-flops trigger on positive-going edges of the input signals, the waveforms of **Fig. 3b** result. These waveforms

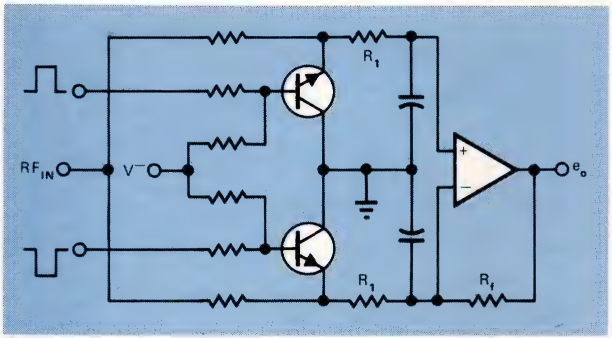


Fig. 4—Phase-sensitive detector is a so-called balanced multiplier, or shunt chopper.

illustrate the multiplying process of the PSD's. After lowpass filtering, the PSD outputs produce the signals v_c (control voltage) and v_c^* (audio output).

Note that when the input and VCO free-running frequencies are equal, $v_c=0$ and v_c^* is at its maximum value. The Q-channel produces an output signal even at very small RF input levels. In other words, there is no threshold effect as in envelope detectors.

Getting inside some of the blocks

The PSD (**Fig. 4**) is a so-called balanced multiplier or shunt chopper. As in all shunt choppers, the open resistance doesn't equal ∞ and the closed resistance doesn't equal zero. However, these nonideal characteristics aren't problem sources. Conservatively estimating open resistance at 100 kΩ gives a signal attenuation of 0.003. Nonzero closed resistance gives rise to a residual voltage level Δv. The output voltage, due to this voltage level, is:

$$\Delta v_o = (\Delta v_1 - \Delta v_2)\cdot\frac{R_f}{R_1} + \Delta v_1$$

Thus, when $\Delta v_1 = \Delta v_2$, an offset voltage Δv_1 will appear at the op-amp output. This offset voltage has little consequence, since the dc output voltage level of the op amp is adjustable. Secondly, due to the inverted transistor configuration, the magnitude of Δv_1 is only of the order of 1 mV or less.

Low-pass filters follow the choppers. These filters have a 10 kHz cutoff frequency and remove most HF components from the PSD outputs. The filtered signals are then applied to the summing op amp, which in turn supplies the input voltage to the loop filters.

The loop filter (**Fig. 5a**) is of the lead-lag type. Such an arrangement allows some of the higher frequency components to build up a correcting voltage in the filter. Prior to capture, the VCO is therefore pulled towards the input frequency. When this happens, more correcting voltage is developed and a snowballing action takes place until the VCO snaps into synchronization with the input signal. The transfer function of this filter is:

$$\left|\frac{e_o}{e_i}\right| = \sqrt{\frac{1+\beta^2(\omega\tau)^2}{1+(\alpha\beta)^2(\omega\tau)^4+(1+\alpha+\beta)^2(\omega\tau)^2}} \qquad \textbf{(1)}$$

where $\alpha = 0.0373$
$\beta = 0.1$
$\tau = 2.2\times10^{-3}$

Keeping things in phase

Based on the bootstrap principle, a linear sawtooth oscillator is the heart of the VCO (**Fig. 6**). Tuning capacitor C is linearly charged to a voltage level set by the reference input of a comparator. Voltage across C comes from the source of a source follower, Q_2, and is dc coupled to the signal input of the same comparator. When this voltage reaches the set reference level, the comparator changes state, providing base current to saturate discharge transistor Q_3. When C is properly discharged, the comparator changes state again. Q_3 is cut off, enabling C to recharge. The process then repeats.

The sawtooth voltage at the source of Q_2 also feeds a differentiating network, which lowers the average dc level of the sawtooth wave to 0V. A second comparator, having the reference input set at 0V, then produces a square-wave output of the same frequency as the sawtooth. A single inverter shapes this square wave to adapt it for triggering FF_1. Similarly, two inverters trigger FF_2. Thus, the flip-flop outputs (**Fig. 6b**) switch the transistors in the PSD's. Phase quadrature between the outputs of the two flip-flops is preserved at all operating frequencies.

Varying the current in current source Q_1 controls the VCO frequency. If control voltage v_c goes more positive, drain current i_2 increases. Charging current i_1 decreases accordingly, there-

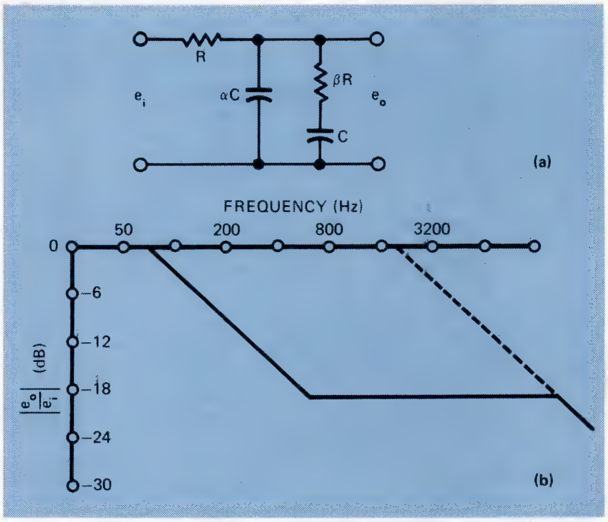


Fig. 5—Lead-lag arrangement of the loop filter allows high-frequency components to aid in VCO synchronization.

by lowering the VCO frequency. From **Fig. 6**, the sawtooth frequency can be expressed, in terms of circuit parameters, as:

$$f = \frac{V^+ - V_s - v_c \cdot \dfrac{R_2}{R_1}}{C(R_2 + R_3)\,(V_r - V_{gs} - V_s)} \qquad \textbf{(2)}$$

where V_s equals the saturation level of Q_3.

By differentiating **Eq. 2**, the VCO conversion gain K_0 can be derived. A factor two has to be accounted for since circuit operation is based on half the sawtooth frequency. Thus:

$$2K_0 = \frac{d\omega}{dv_c} = -2\pi \cdot \frac{R_2/R_1}{C(R_2 + R_3)\,(V_r - V_{gs} - V_s)} \qquad \textbf{(3)}$$

Taking $V_r - V_{gs} - V_s = 1.7V$ and substituting component values:

$K_0 \approx 5 \times 10^7$ rad/sec/volt with C=100 pF ($f \approx 1.6$ MHz)

$K_0 \approx 10^7$ rad/sec/volt with C = 470 pF ($f \approx 0.5$ MHz)

In **Eqs. 2** and **3**, secondary effects, such as parasitic capacitances, and loading effects have not been included, since we do not intend to present a detailed mathematical analysis. It should be noted, however, that the positive supply voltage, V^+, is a parameter in **Eq. 2**. Good circuit stability, therefore, mandates the use of a well stabilized supply.

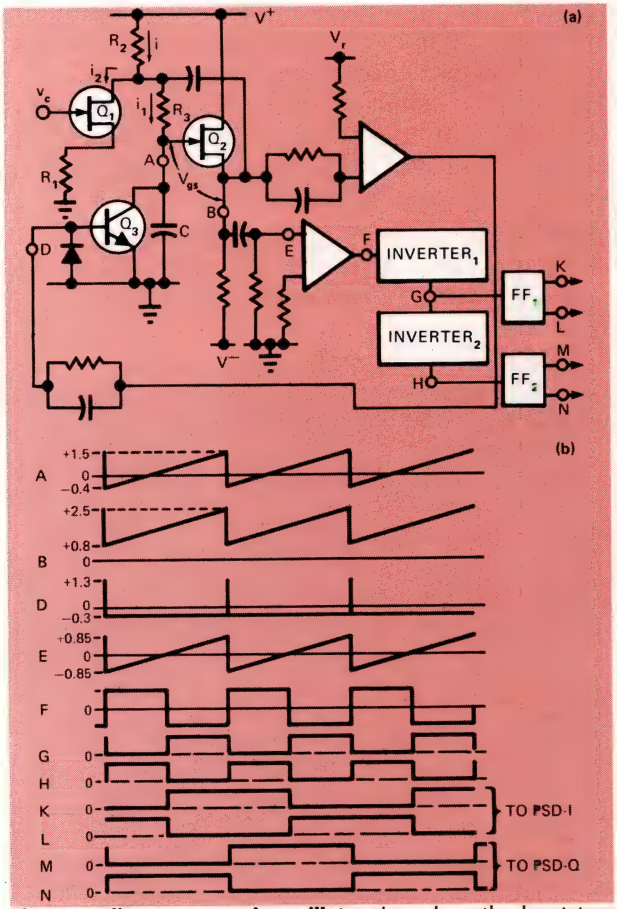


Fig. 6—A linear sawtooth oscillator, based on the bootstrap principle, is the heart of the VCO.

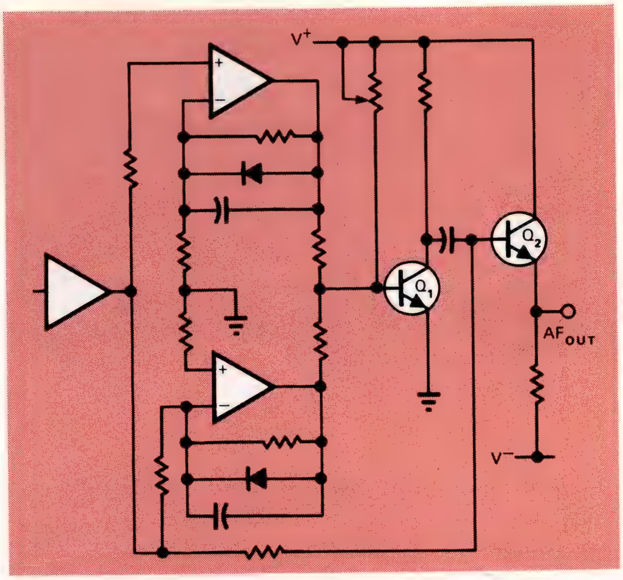


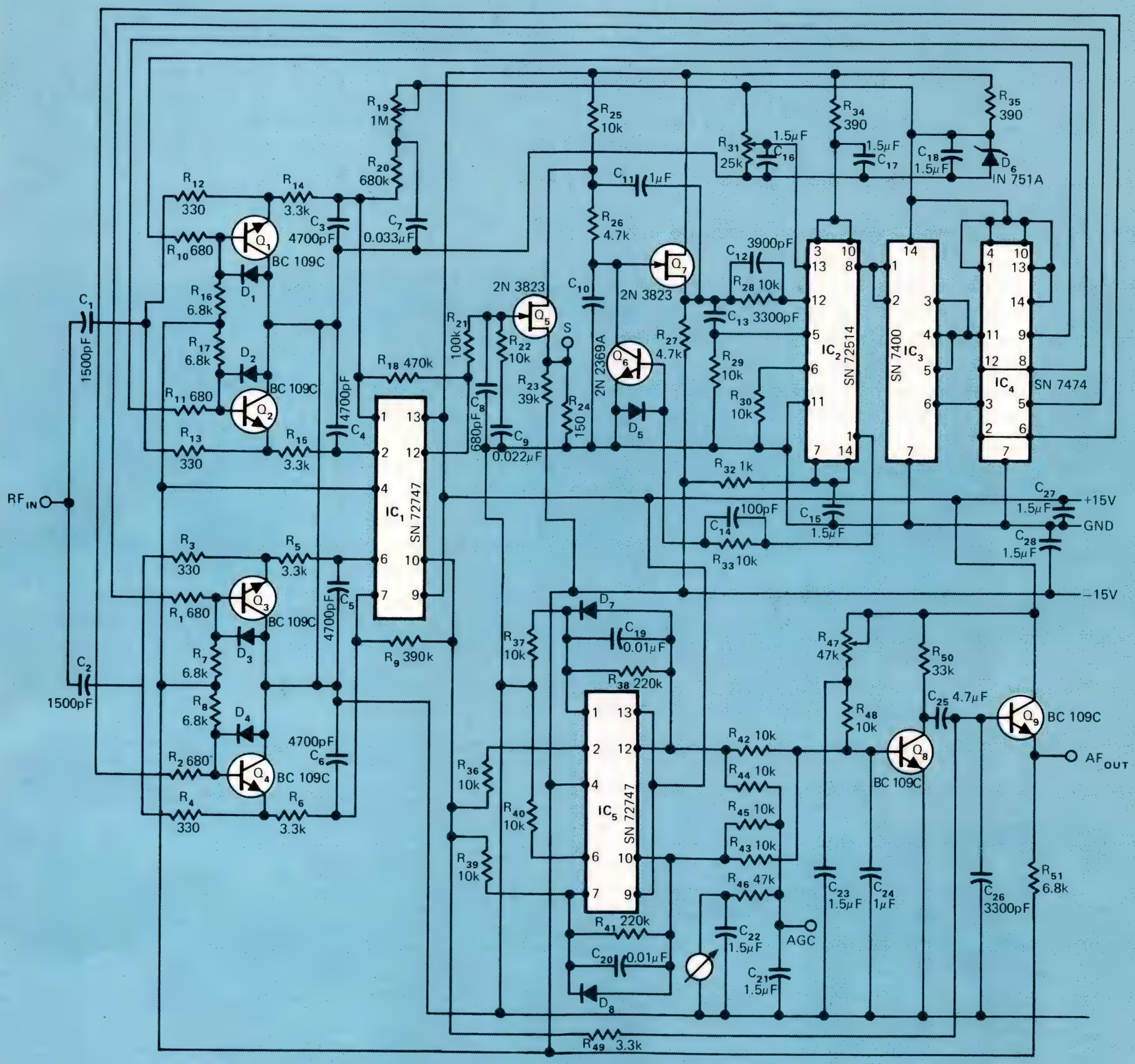
Fig. 7—Muting circuit suppresses annoying whistles heard prior to capture.

Hold the whistles down

The muting circuit (**Fig. 7**) suppresses heterodyne whistles when tuning across the band. One of the frequency components of the PSD's is the difference between RF input and VCO. When this difference frequency is high enough, it will be almost entirely filtered out and go unnoticed. However, when tuning to a station, the VCO frequency approaches the station frequency and the difference frequency will enter the passband of the audio filter. As a result, an annoying whistle is heard prior to capture.

To suppress these whistles, the audio signal is rectified and amplified and the rectified voltage used to control a threshold circuit. This circuit is nothing but a transistor switch that passes or blocks the audio signal. Two rectifying amplifiers are used; one which amplifies positive signals, and one which amplifies negative signals. The reason for this arrangement becomes apparent from **Fig. 3**. Depending upon the state of the flip-flops when the circuit is turned ON, the phase relationship between RF input and FF_2 outputs can either be as shown or exactly opposite. Because of this unpredictable state, you have to account for both possibilities.

When the RF frequency is just outside the receiver's capture range, either one of the amplifiers will produce a negative voltage level. As this level is insufficient to cut transistor Q_1 OFF, the saturated transistor will block the audio output. As the receiver is correctly tuned, the maximum negative-voltage level will be produced. By adjustment of the muting level, this negative level can be made to cut Q_1 OFF, and audio information is allowed to pass to the output.



NOTE: D_1, D_2, D_3, D_4, D_5, D_7, D_8 = High-speed Ge types

Fig. 8—Despite its seeming complexity, the PLL receiver requires only two operational adjustments.

Putting it all together

Fig. 8 shows the circuit diagram of the complete experimental receiver. Measurements on this circuit were made using an RF generator with adjustable output level and 50Ω output impedance. A fixed modulation of 1 kHz, and 30% modulation index, could be switched ON or OFF. During all measurements, the muting circuit was disabled.

Adjustment of the reference input of IC_2 is a 2-step procedure. First, potentiometer R_{19} is adjusted such that the voltage at the source of Q_5 (point S) equals 0V. With a fixed 470 pF tuning capacitor inserted, and the RF frequency set to 540 kHz, the reference voltage is adjusted (R_{31}) until capture is observed on an oscilloscope.

As is to be expected in **Eq. 2**, VCO frequency varies almost inversely with capacitance value due to the linear operation of the sawtooth circuit. The outcome of our measurements suggest the addition of an RF amplifier preceding the PLL. A moderate amplifier gain of 50-100 seems adequate to obtain a 5 to 10 μV sensitivity.

Designs of various low-noise amplifiers can be found in the literature. Of these, an FET amplifier seems to offer the best features. In order to block large interfering signals, preselection should be incorporated in the amplifier. Preselection, however, implies tracking of RF and sawtooth frequency. In an LC preselection circuit, tuning frequency varies as the inverse of the square root of capacitance value, so that perfect tracking of these two signal frequencies is not possible. Fortunately, the preselection circuit can be rather wideband, so this problem does not seem insurmountable.

Because of the large range of input signal levels, AGC will be required. As indicated in **Fig. 8**, the combined output of the comparators in IC_5 is available as an AGC voltage to control the gain of the RF amplifier. This voltage can also drive a tuning meter that deflects to maximum value when tuning is correct. An alternative tuning indicator would be a balance meter connected to the source of Q_5, indicating zero for correct tuning. However, since these voltage excursions at the source are quite small, dc amplification of the source voltage will be necessary to operate such a meter.

Other possibilities exist

This design represents just one implementation of a PLL-AM receiver. It demonstrates the potential of phase-locking techniques in this area of electronics. No optimum design claims are made. Improvements and additions can be visualized, such as the use of chopper transistors in the PSD's, a lock-range limiter circuit, etc. Furthermore, a different VCO, such as an astable multivibrator, may work as well, and the muting feature could be implemented by different threshold circuits. ☐

Author's biography

Thomas Mollinga writes from more than a pure academic background. Before joining the lecturing staff at Technical College in 1971, he spent the previous 15 years in industry. Following an 8-year stint with Burroughs Corp. in Pasadena, CA, he worked on weapon control systems for HSA, Hengelo in the Netherlands. A graduate of the University of Amsterdam, with degrees in Math and Physics, he has been granted eight patents. When time permits, Tom enjoys literature, history and classical music.

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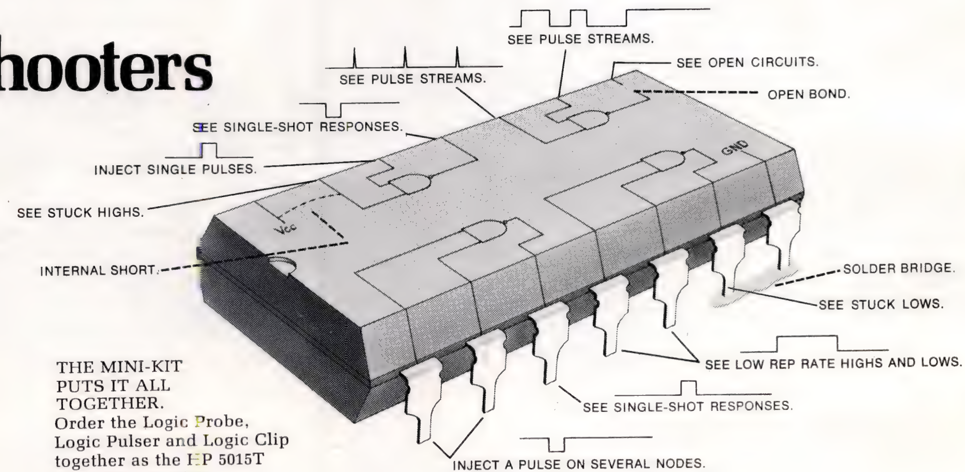

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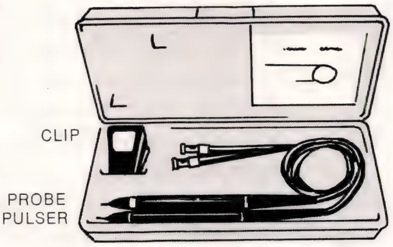

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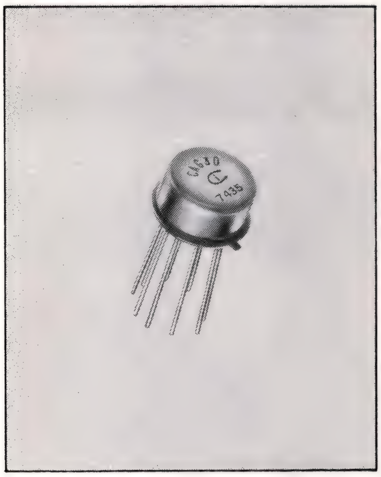

The CAG30 is a low cost general purpose FET switch capable of switching analog signals up to ±10 volt. This switch can be controlled from TTL or DTL and is designed with high logic noise immunity. (typically 1.0 V). Additional flexibility is provided by an input comparator stage which allows the switch to be activated directly from an analog voltage. Parts can be processed to MIL-STD-883 Level A, Level B, or other special requirements.

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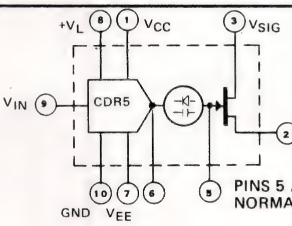
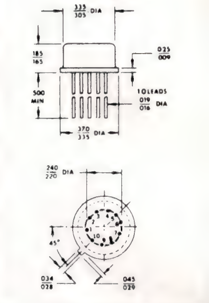


PINS 5 AND 6 ARE NOT USED IN NORMAL OPERATION (LEAVE OPEN)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	T_{OPR}	−55	to	+125	°C
Storage Temperature	T_{STG}	−55	to	+150	°C
Logic Supply Voltage	V_L	+4.5	to	+5.5	V
Logic Input Voltage	V_{IN}	0	to	V_L	V
Positive Supply Voltage	V_{CC}	0	to	+18	V
Negative Supply Voltage	V_{EE}	−18	to	−7	V

TO−100



The CAG30 is a low cost general purpose FET analog gate capable of switching up to ±10V signals directly from DTL or TTL while providing high logic noise immunity (typically 1.0V). The use of a monolithic switching circuit as a driver has the advantage of small size and full military temperature range at low cost. The CAG30 turns off faster than it turns on to allow multiplexing without shorting.

Logic 1 (≥ 2.0V) closes contacts
Logic 0 (≤ 1.0V) opens contacts

ELECTRICAL CHARACTERISTICS: $T_A = +25°C$; $V_L = +5.0V$; $V_{B-} = -18V$; $V_{B+} = +18V$ (Unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Signal Range	V_{SIG}	See Note (1)	−10		+10	V
Drain-Source On-Resistance	Rds	I_D = 1mA, V_{IN} = 2.0V			60	Ohms
Drain-Gate Capacitance	Cdgo	Vdg = 10V, I_S = 0, f = 140KHz		6		pf
Source-Gate Capacitance	Csgo	Vsg = 10V, I_D = 0, f = 140KHz		6		pf
On Current	I_D (on)	V_{DS} = 2.0V, V_{IN} = 2.0V		20		mA
Drain Cut-off Current	I_D (off)	V_{DS} = -10V, V_{IN} = 1.0V			1.0	nA
Source Cut-off	I_S (off)	V_{SD} = -10V, V_{IN} = 1.0V			1.0	nA
Logical "1" Input Voltage	V_{IN} (1)		2.0	1.5		V
Logical "0" Input Voltage	V_{IN} (0)			1.5	1.0	V
Logical "0" Input Current	I_{IN} (0)	V_{IN} = 1.0V			10	µA
Logical "1" Input Current	I_{IN} (1)	V_{IN} = 2.0V			30	µA
Logic Supply Current	I_L			1.8	4	mA
Positive Supply Current	I_{CC}			3.5	5	mA
Negative Supply Current	I_{EE}			3.5	5	mA
Propagation Delay Time to Logical 0	T_{pd}^0	C_L = 20pf, R_L = 1K			0.5	µS
Propagation Delay Time to Logical 1	T_{pd}^1	C_L = 20pf, R_L = 1K			1.0	µS
Total Power Dissipation	P_T			75	150	mW

NOTE 1) V_{IN} limits are determined by the V_{CC} and V_{EE} voltages.
V_{IN} min. = (V_{EE} + 8V) and V_{IN} max. = (V_{CC} −2V)
Ex. V_{EE} = −8V, V_{CC} = +8V, V_{IN} = 0 to +6V

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Here's your chance to learn how to write for publication. September 20, pg. 24 (N)

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When your system's data rates differ, it's time for a microprocessor. November 20, pg. 57 (F)

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Sine/square/triangle generator requires only 3 IC's. August 20, pg. 96 (C)

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Submillimeter waves achieved with lasers. July 20, pg. 12 (N)

Temperature measurement method requires no reference. August 5, pg. 78 (C)

Testing and adjusting analog dividers. July 5, pg. 59 (F)

Today's system concepts demand instruments be made intelligent. September 20, pg. 40 (F)

Indicating limiter uses low cost IC's for exotic operation

Leonard M. Smithline
Lansing Research Corp., Ithaca, NY

Combining the extremely flat plateaus of zener limiters with the programmability and precise limit selection of resistive ratio limiters makes this circuit unique.[1] I also exploit the current-limiting feature of popular 741 and 307 op amps in my shunt-type limiter. Intended for use in over-voltage protection applications, the circuit indicates when it is in either clipping state. In addition, the clipping levels in both directions are thermally stable.

Without the limiter (**Fig. 1**), the circuit would consist of the 307 op amp and its load. The original signal path is shown as a heavy line, added onto it is the limiter circuitry consisting of four transistors, eight resistors and two LED's.

When the op-amp output, V, equals zero, current source Q_1 supplies a current which Q_3 sinks. The voltage drops across R_2 and R_3 back-bias Q_2 and Q_4, turning them OFF. Thus, until V goes positive enough to turn Q_4 ON or negative enough to turn Q_3 ON, the op amp sees no additional load due to the limiter circuitry.

I will delinate first quadrant operation; third quadrant operation is identical.

When V becomes sufficiently positive, Q_4 turns ON, loading the op amp. A small increase in V beyond this point is greatly amplified by Q_4, causing the op amp to current limit. At this point, further increase in V is not possible so the output level remains limited.

The 307 current limit (20 mA) is a perfect value for driving LED's. Therefore, by having Q_4 draw its current through D_2, we acquire perfectly synchronized indication about entrance into a limiting state.

To turn Q_4 ON, V must be greater than V_p':

$$V_p = I_3R_3 + V_{BE} \tag{1}$$

V_p is the positive threshold and V_{BE} is the transistor base-emitter drop. I_3, the Q_3 collector current, may be expressed as:

$$I_3 = \frac{V_S - V_B - V_{BE}}{R_4} \tag{2}$$

where V_S and $-V_S$ are the two supply voltages, and V_B and $-V_B$ are the base voltages of Q_1 and Q_3, respectively. In my circuit, V_B is generated by a resistive divider. Combining (1) and (2), and making $R_3 = R_4$ so that the thermally sensitive V_{BE} terms drop out, we get:

$$V_p = V_S - V_B \tag{3}$$

In **Fig. 1**, $V_p = 2.0V$.

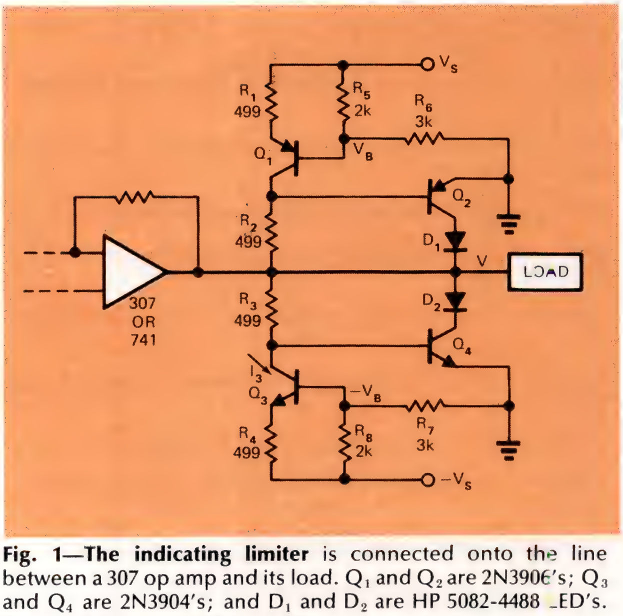

Fig. 1—The indicating limiter is connected onto the line between a 307 op amp and its load. Q_1 and Q_2 are 2N3906's; Q_3 and Q_4 are 2N3904's; and D_1 and D_2 are HP 5082-4488 LED's. We used V_S = 5V and V_B = 3V.

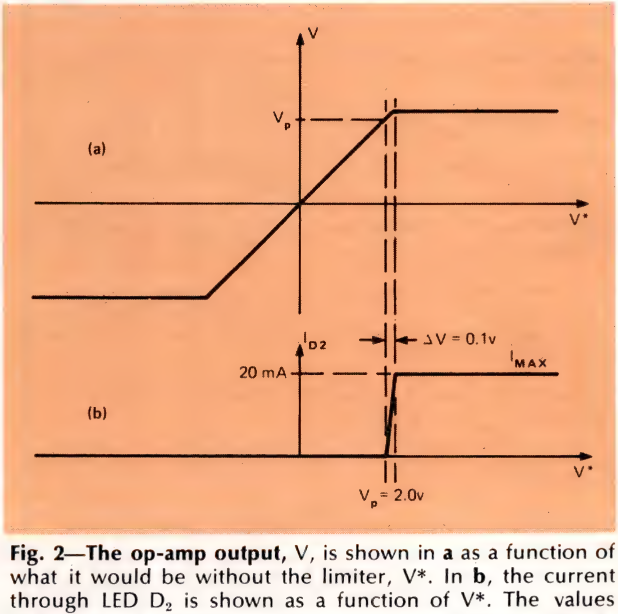

Fig. 2—The op-amp output, V, is shown in **a** as a function of what it would be without the limiter, V*. In **b**, the current through LED D_2 is shown as a function of V*. The values indicated in both graphs are for components shown in **Fig. 1**.

To attain the nonloading feature, we must have $R_1 = R_2 = R_3 = R_4$.

After turning Q_4 ON, V continues to increase by ΔV until the current drawing by Q_4 is the op-amp current limit, $I_{MAX.}$.

$$\Delta V = \frac{I_{MAX}R_3}{\beta}$$

Where β is the forward current gain of Q_4. V_p and ΔV are illustrated in **Fig. 2**; ΔV in the circuit of **Fig. 1** is about 100 mV.

By making β large and R_3 small, ΔV can be made extremely small. However, a 5 to 10% increase in linearity after the LED's will give warnings of limiting; R_3 and β can be chosen to achieve this.

V_B and $-V_B$ may be derived from low impedance sources to achieve programmability. Other ramifications include replacing D_1 and D_2 by optoisolators to drive logic or alarms. ☐

Reference

1. G. Tobey, J. Graeme, L. Huelsman, "Operational Amplifiers—Design and Applications," McGraw-Hill, 1971.

To Vote For This Circuit
Circle 160

Program Optimizes piecewise-linear function modeling

Dennis Feucht,
Tektronix, Inc., Beaverton, OR

In the FOCAL program, it is necessary only to specify the number of segments desired in approximating the function and the percent distribution of displacement error among the segments. The program does the rest by determining the breakpoint locations for approximating a given monotonic function between two established input values (x-values) of the function. The following example illustrates this.

The function to be modeled is inputed as:

20.10 SET GX = (function in terms of x)

Then take the derivative of the function and solve for x. If, for example, f(x) = ln x, then f'(x) = 1/x, and [x = 1/f' (x)]. Now label f' (x) as X and x as XM, and input as:

21.10 SET XM = 1/X

The requested variables are:

XB = Lower Bound of interval over which function is to be approximated.
XE = Upper Bound
Number of Segments = Number of Segments.
% Distribution of Error = The allowed difference in maximum displacement error among the segments. The absolute error will be within ±% distribution of error for all segments and is printed out along with the breakpoint locations.

The sample run that follows is for a 5-segment approximation of a sine wave in the first quadrant.

```
10. 05 E
10. 10 C TO DEFINE F(X), TYPE: 20.10 SET GX=
10. 15 C TO DEFINE THE DERIVATIVE OF F(X) SOLVED
        FOR X, TYPE: 21.10 SET XM=
10. 20 ASK !, "XB='', XB, !, "XE=", XE, !, "NUMBER OF
        SEGMENTS=", N, !
10. 25 ASK "% DISTRIBUTION OF ERROR=", ED, ! !
10. 30 SET J=1
10. 35 SET LB=0
10. 40 SET X2=XE
10. 45 SET X1=XB
10. 50 DO 15.0
10. 52 SET ER=E
10. 55 SET YE=Y2
10. 57 SET X2=XB
10. 60 IF (J-N)10.70, 10.65, 10.85
10. 65 IF   ((FABS((Y2-YE)/(YE+Y2)/2))* 100-ED)13.05,
        10.70, 10.70
10. 70 SET UB=E
10. 75 SET ER=ER-(UB-LB) /2
10. 80 GOTO 10.95
10. 85 SET LB=E
10. 90 SET ER=ER+(UB-LB) /2
10. 95 SET X1=XB

11. 05 SET J=1
11. 10 GOTO 16.25

13. 05 TYPE "BREAKPOINTS ARE:", !
13. 10 FOR I-1, N-1; DO 14.0
13. 15 TYPE !, "SEGMENT ERROR=", ER
13. 20 TYPE ! !
13. 25 QUIT

14. 05 SET X=B(I)
14. 10 DO 20.0
14. 15 SET YO=GX
14. 20 TYPE "X=", B(I)," Y=", YO, !

15. 05 SET X=X2
15. 10 DO 20.0
15. 15 SET Y2=GX
15. 20 SET X=X1
15. 25 DO 20.0
15. 30 SET Y1=GX
15. 35 SET S=(Y2-Y1)/(X2-X1)
```

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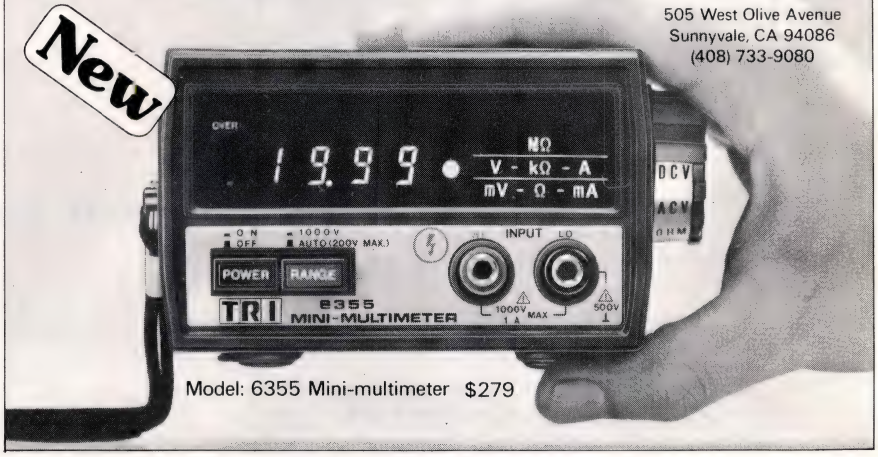

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For more information, Circle No. 26

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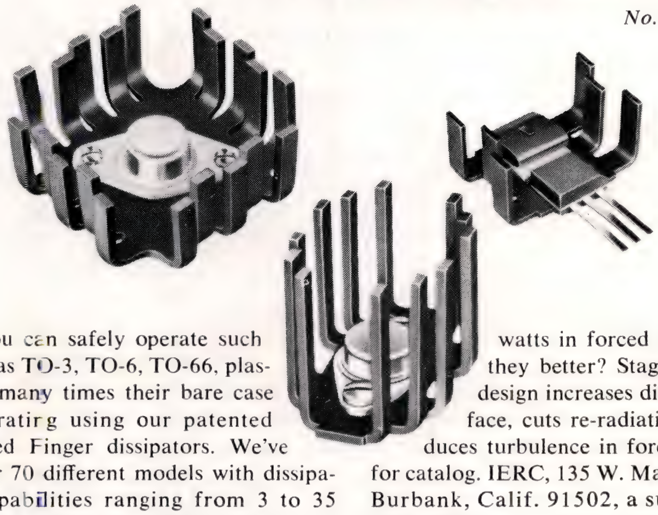

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IERC DCA **Heat Sinks**

For more information, Circle No. 28

```
15. 40 SET X=S
15. 45 DO 21.0
15. 50 SET Z=XM
15. 55 SET X=XM
15. 60 DO 20.0
15. 65 SET YZ=GX
15. 70 SET LZ=Y1+S* (Z-X1)
15. 75 SET E=FABS(YZ-LZ)

16. 05 IF (X2-XE)16.10, 10.60, 10.60
16. 10 SET B(J)=X2
16. 15 SET J=J+1
16. 20 SET X1=X2
16. 25 SET X2=XE
16. 30 DO 15.0
16. 35 IF((FABS(E-ER)/ER* 100-ED)16.05, 16.40, 16.40
16. 40 IF (E-ER)16.55, 16.05, 16.45
16. 45 SET X2=X2-FABS(X2-X1) /2
16. 50 GOTO 16.30
16. 55 SET X2=X2+FABS(X2-X1) /2
16. 60 GOTO 16.30
20. 10 SET GS=FSIN(X)
21. 10 SET XM=1. 57080-FATN(X/FSGT(1-X+X))
```

```
G

XB=0

XE=1.57080

NUMBER OF SEGMENTS=5

% DISTRIBUTION OF ERROR=5

BREAKPOINTS ARE:
X=          0.5380          Y=          0.5124
X=          0.8870          Y=          0.7752
X=          1.1950          Y=          0.9302
X=          1.4769          Y=          0.9956
SEGMENT ERROR=     0.0099                  □
```

To Vote For This Circuit
Circle 161

Rectangular-to-polar coordinate conversion is simple

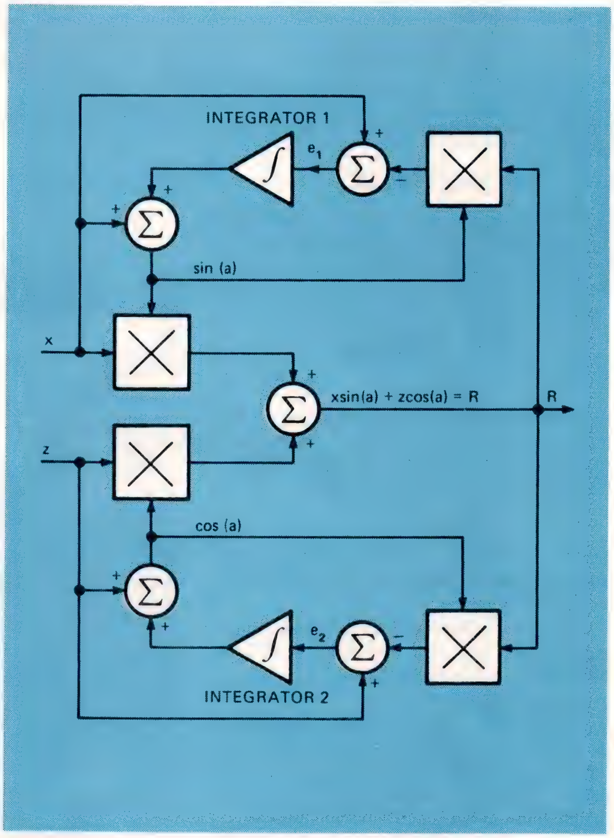
William H. Licata
Naval Ordnance Lab., Silver Springs, MD

This circuit converts analog signals representing the rectangular coordinates of a vector, to analog signals representing the polar coordinates of the same vector. The desired signal is the phase angle of the vector, a, which is to be compared with a reference phase value a_0, generating the error signal $a-a_0$.

Actually, instead of generating a signal proportional to a, the circuit generates a signal proportional to sin(a) and one proportional to cos(a). The signal $\sin(a-a_0)=\sin(a)\cos(a_0) - \sin(a_0)\cos(a)$ is then used as an approximation of $a-a_0$. Identical and coupled nonlinear feedback loops are the essential system ingredients.

Assume that the output of integrator 1 is $\sin(a)-x$ and the output of integrator 2 is $\cos(a)-$ Error signals e_1 and e_2 equal zero if $x = R\sin(a)$ and $z = R\cos(a)$, where R is the magnitude of the vector. This means that the two integrators hold at the desired values. However, if $x > R\sin(a)$, then e_1 is positive, which drives the integrator output positive and increases the estimate of sin(a). If $x < R\sin(a)$, the error signal is negative, which decreases the estimate of sin(a). Thus, the feedback works in the proper direction.

When constructed, the prototype circuit demonstrated a high degree of stability. The output converges rapidly to the correct answer. Obtainable accuracy depends on the electronics used, but 1% of full-scale has been achieved. □



Two nonlinear feedback loops produce the desired function while saving the cost of an analog resolver. To further decrease cost, the circuit was built using one multiplier in a time-shared mode.

To Vote For This Circuit
Circle 162

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We'll send you our new System 823 literature or ask for a DIT-MCO representative to show you how a System 823 relates to your test needs. He'll show you how to perform tests faster, more simply, and save money too!

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DIT-MCO INTERNATIONAL
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Telex Number 42-6149

European Technical Representative, Radix House,
Central Trading Estate, Staines, Middlesex,
TW18-4-XA, England, Telephone (0784) 51444
Telex Number 935023

For more information, Circle No. 29

NEW! MINI-BREADBOARD BUDGET KIT FOR THE ECONOMY-MINDED EXPERIMENTER . . .

Proto Board 100

Patent Pending
Made in USA

Here's a low cost, big 10 IC capacity breadboard kit with all the quality of QT Sockets and the best of the Proto Board series. Complete down to the last nut, bolt 'n screw. Includes 2 QT-35S Sockets; 1 QT-35B Bus Strip; 2 5-way binding posts; 4 rubber feet; screws nuts, bolts and easy assembly instructions. Order off-the-shelf today from CSC or local distributor. Charge: BAC, MC, AX. Write for free catalog. Free English/Metric Slide Rule with each order. Dealer inquiries invited.

Complete Kit:
19^{95}
Add $1.50 shipping/handling.
Foreign orders add 15%.
Prices subject to change

CSC Continental Specialties Corp.
Box 1942, New Haven, CT 06509 • 203/624-3103
W. Coast Off.: Box 7809, S. Fran., CA 94119 415/383-4207
Canada: Available thru Len Finkler Ltd., Ontario

For more information, Circle No. 30

IT'S HERE. ANALOG DEVICES' $39 12-BIT IC DAC.

Introducing the AD562 – the most accurate, lowest cost 12-bit DAC on the market.

It gives you guaranteed monotonicity over the full operating temperature range; a maximum total error as low as 1/4LSB (0.006%) at 25°C; a 3ppm/°C maximum gain temperature coefficient; and comes in a hermetically sealed, 24-pin DIL package.

You can specify the AD562 guaranteed for operation over three temperature ranges: 0 to +70°C, −25 to +85°C, and −55 to +125°C.

Prices start at $39 in hundreds.

For more information, send for the data sheet. Or call Analog Devices Semiconductor, Norwood, MA 02062.
East Coast, (617) 329-4700.
Midwest, (312) 297-8710.
West Coast, (213) 595-1733.

ANALOG DEVICES

For more information, Circle No. 31

Calculate large powers using a 4-function calculator

Charles R. Martin
IBM Corp., Kingston, NY

This method is my variation of "Get the most from your 4-function calculator" by Henry Morris, EDN, July 5, 1974.

Owners of 4-function calculators with a constant feature are probably well aware that quantities can be raised to powers by pressing the times (×) key and then repetitively pressing the equals (=) key.

I find it easier and more accurate to calculate large powers using powers of 2. In fact, many calculators that do not have the constant feature are capable of squaring the displayed number. Simply press first the (×) then the (=) key. For example, to raise 1.008125 to the 240th power:

$$(1.008125)^{240} = (1.008125)^{(128+64+32+16)}$$

$$= (1.008125)^{128} \times (1.008125)^{64} \times (1.008125)^{32} \times (1.008125)^{16}$$

The calculating sequence, beginning with 1.008125 entered, is: (×) (=) (×) (=) (×) (=) (×) (=), and write down the result, which is $(1.008125)^{16}$. Then (×) (=) and write down the result, $(1.008125)^{32}$. Then (×) (=) after which $(1.008125)^{64}$ is displayed. Finally, (×) (=) after which $(1.008125)^{128}$ is displayed. Then the four factors are multiplied out to yield a result of 6.9734838.

This method is easier than pressing the (=) key 239 times and is also more accurate, since simple calculators do not round in the low-order digit, but truncate. The more multiplication operations that are performed during a given calculation, the larger the truncation error will be.

This type of calculation can also be used to determine long-term compound interest. For example: Find the monthly payment for a $30,000, 20-year, 9-3/4% mortgage:

$$MP = \frac{i(1+i)^N}{(1+i)^N - 1} \times P$$

where i = monthly interest rate = 0.0975 ÷ 12 = 0.008125
N = term in months = 240
P = initial principal = $30,000

$$MP = \frac{(0.008125)(1.008125)^{240}\,(30000)}{(1.008125)^{240} - 1}$$

We have already found $(1.008125)^{240}$ to be 6.9734838. The monthly payment then is calculated to be $284.56. ☐

To Vote For This Circuit
Circle 163

Readers have voted:

Henry D. Olson winner of the May 20, 1974 U.S. Savings Bond Award. His winning circuit is "Automatic battery charger shuts itself down." Mr. Olson is with Stanford Research Institute, Menlo Park, CA.

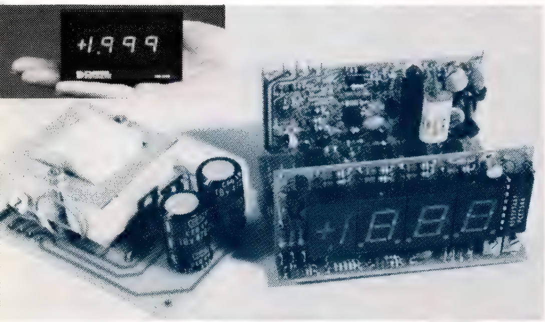
David J. Beckwitt winner of the July 5, 1974 U.S. Savings Bond Award. His winning circuit is "Ac ohmmeter provides novel use for opto-isolators." Mr. Beckwitt is with Soiltest, Inc., Baraboo, WI.

J. Daniel McCranie winner of the August 20, 1974 U. S. Savings Bond Award. His winning circuit is "Sine/square/triangle generator requires only 3 IC's." Mr. McCranie is with Signetics Corp., Sunnyvale, CA.

Richard C. Jaeger (left) and **George A. Hellwarth** winners of the June 5, 1974 U. S. Savings Bond Award. Their winning circuit is "Differential cascode amplifier offers unique advantages." Mr. Jaeger and Mr. Hellwarth are with IBM Corp., Boca Raton, FL.

Large display, smallest case distinguish ac-powered 3-1/2-digit DPM

PROGRESS IN INSTRUMENTATION



Simple multi-pc board construction of Datel's line-powered DM-2115 permits very compact construction, yet good accessibility for service. Note the 0.43-in. light-pipe display. Inset gives an indication of size.

Housed in a LEXAN^{R} case measuring only 1.75×2.25×3 in., the DM-2115 by Datel Systems, Inc., occupies <12 in.^{3}. That makes it the world's smallest ac-powered unit.

But readability hasn't been sacrificed to achieve small size. The DM-2115's 0.43-in. red light-pipe LED display is far easier to read than the 0.27- or 0.3-in. digits usually found on much larger DPM's.

Heat generation is minimal, thanks to a custom designed C-core, strip-wound power transformer. This design also minimizes the external electrostatic and magnetic fields and provides compact dimensions. Power drain of the whole DPM is <3.5W.

The meter accepts ±1.999V true-differential inputs and presents >100 MΩ input resistance. Standard features include autopolarity, overflow display and selectable decimal points, as well as >70 dB CMR from dc to 60 Hz. Accuracy is specified as 0.05% ±1 count, while the TC is <50 ppm/°C (only 5 counts over the temperature range of 0 to 50°C).

Why ac power?

There are several good reasons to consider ac powering (rather than +5V dc logic power) for a small DPM. For one, many simple analytical and research instruments have no logic circuitry, hence they can't provide suitable +5V dc power. Line powering as provided in the DM-2115 saves the expense of a separate supply, as well as the space it would take up. Even more important in some instances, a +5V DPM can add logic noise onto the +5V bus with each conversion. Unless filtered, this noise can be misinterpreted as false codes by the instrument's logic section.

Another point concerns the isolation made possible by ac powering. Unlike +5V dc units that generally have single-ended inputs, the ac-powered unit permits transformer-isolated true differential inputs.

Looking at the other side of the coin, dc powering has its advantages, too. So for those who want +5V dc logic powering, Datel offers models that require only 400 mA max. current. These are wired so that the display circuits can be blanked to reduce the total drain to 120 mA. Using a "press to read" switch, or providing duty cycled operation on +5V power for the display permits efficient battery operation.

Price for an ac-powered DM-2115 without BCD output runs $159. BCD adds $16. Models for +5V dc power sell for $129 without—and $145 with—BCD. Prices include connectors.

Datel Systems, Inc., 1020 Turnpike St., Canton, MA 02021. Phone (617)828-8000.

Circle No. 140

It's bigger than a µP and smaller than a mini—it's a millicomputer

PROGRESS IN COMPUTERS

A full-scale 16-bit bipolar MSI processor, the NAKED MILLI™ bridges the confusing gap between microprocessors and minicomputers. Designed to be cost effective in areas where a microcomputer would otherwise be used, Computer Automation's millicomputer offers compatible expandability upward through the full range of minicomputer performance. It also provides a powerful instruction set and flexible high-speed I/O. Thus, this new breed of computer fills the vacuum between a micro and a mini and overlaps each.

The bare facts

The Naked Milli LSI-3/05 lies on a single half-card that measures 7-1/2 × 15 in. This smallest and lowest cost processor of the LSI family is electrically and mechanically interchangeable with other members of the family. Also, all programs written for the "Milli" will run on the larger LSI family members. Architecture is a full 16-bit computer that includes 8 addressing modes, 16-bit word and 8-bit byte processing and standard DMA.

Slightly slower than most mini's but faster than most micro's, this processor may offer you the best solution to your application. Operating with a set of 93 microcoded instructions, the machine can perform a 16-bit add function in 6 μsec. These instructions feature single-word format, complete logic instructions and a large repertoire of commands to reduce programming time, conserve memory and increase throughput. Macro's are available to perform operations not implemented in firmware.

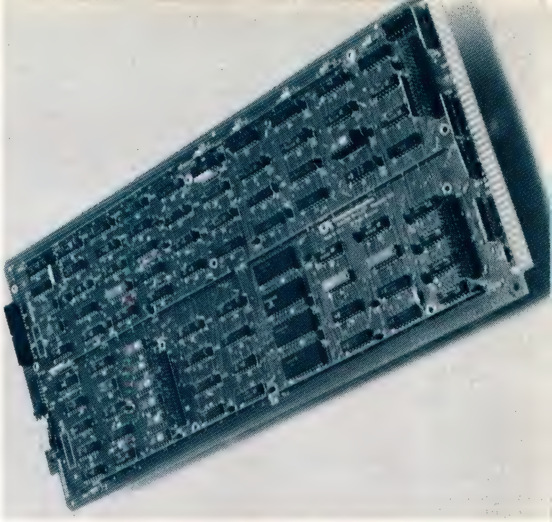
Easy in, easy out

The I/O structure is one of the Naked Milli's strong points. The user does not have to add hardware around the machine to get in and out effectively. Because it is a member of a large family of computers, the millicomputer user has available a wealth of memory and I/O options that simply do not exist for microcomputers. Now the user can concentrate on designing his product and not on producing peripheral interfaces.

Further contributing to the Naked Milli's cost-effective performance is the availability of a new very low-priced universal interface, which Computer Automation has developed. This distributed I/O system operates with intelligent cables, each containing a microcoded Pico-Processor™ that can communicate with most devices and peripherals. Thus, the system eliminates the need for expensive, single-use interfaces.

Meet Milli's mates

Extensive system support includes 3 chassis types, 2 power supplies and 2 types of consoles. Memory can be core, RAM, ROM and pROM in sizes from 1k to 32k bytes/memory module. Software encompasses loaders, utilities, a debug package, the OMEGA conversational assembler/editor and a Real-Time Executive. Programming support is provided by the LSI-2 based Disc Operating System.



The NAKED MILLI™ bridges the mini-micro gap, offering upward-compatible flexibility and the most important features of minicomputers, yet it prices competitively with microcomputers.

Standard hardware features include vectored priority interrupts and the LSI "maxibus" I/O systems. These supply separate parallel bus lines for data, command, device address, interrupt, status and control information. Options include real-time clock, power/fail restart, autoload and teletype/CRT serial interface.

The processor, priced competitively with microprocessors, costs $295 for single units. Delivery is 30 days ARO.

Computer Automation Inc., 18651 Von Karman Ave., Irvine, CA 92664. Phone(714)833-8830.

Circle No. 141

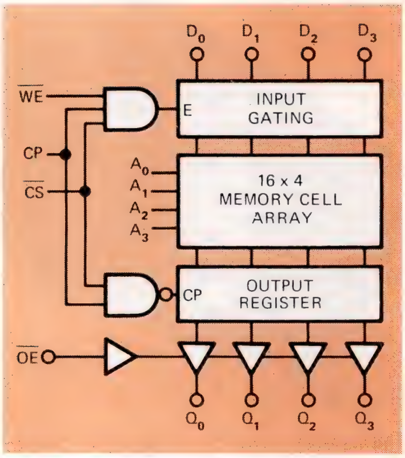
LSI circuits expand the 34000 series Isoplanar CMOS family

PROGRESS IN SEMICONDUCTORS

It has only been a year since Fairchild introduced its first SSI Isoplanar CMOS circuits, but the firm's expertise and confidence in the 34000 family is clearly revealed in the introduction of four new large-scale integration devices.

Available now are the 34702 programmable bit-rate generator and the 34720 256-bit RAM. Available in March will be the 34710 16×4-bit clocked RAM and the 34731 quad 64-bit shift register.

As Dr. Thomas A. Longo, vice president and group general manager of Fairchild's Integrat-



Increased sophistication of the newest members of the 34000 series is indicated by this block diagram of the 34710 16×4 clocked RAM with 3-state output register.

ed Circuits group, explained, "This follows our strategy of bypassing the first-generation metal-gate CMOS technology to provide a completely Isoplanar family of elements featuring standardized characteristics throughout."

Joining the LSI generation

The 34702 programmable bit-rate generator provides the necessary clock and control signals for digital data communication systems. It generates all 13 commonly used bit rates using an on-chip oscillator and an external crystal. One 34702 can control up to eight output channels. Price is approximately $10 in thousands.

The 34720 RAM is organized as 256 words by 1 bit and features complete on-chip decoding with both true and complementary 3-state outputs. The device operates over 3 to 15V; at 10V, typical access time is 80 nsec. Housed in a 16-pin DIP, the 34720 is similar in function and performance to the Philips GZF 1400. Price also is in the $10 range (1000's).

The 34710 RAM is a high-performance memory optimized for register applications. Its 16 word by 4-bit static read/write memory feeds a clocked output register. Bus-oriented, 3-state outputs are provided, and the device is furnished in an 18-pin package.

The 34731 provides four static 64-bit shift registers which operate from dc to 4 MHz. Each section is independent, with separate clock, input and output, and can drive TTL logic directly. Package is a 14-pin DIP.

Pricing for the 34710 and 34731 has not yet been established.

Fairchild Camera and Instrument Corp., 464 Ellis St., Mt. View, CA 94024. Phone(415)962-3800.

Circle No. 142

No-strip mass termination system helps flat-conductor cable take hold

PROGRESS IN INTERCONNECT HARDWARE

Requiring no preliminary cable preparation, Elco's Flattac^R connecting system makes the mass termination of flat-conductor cable completely practical. The usual stripping, indenting, welding or soldering operations are completely eliminated. Instead, the only steps needed are cutting the cable to length and mass-crimping the contracts.

It should be noted that only flat-conductor cable or flexible etched circuitry are suited for use with Flattac. Round-conductor "ribbon" cable (round wires in a flat insulating ribbon) is not.

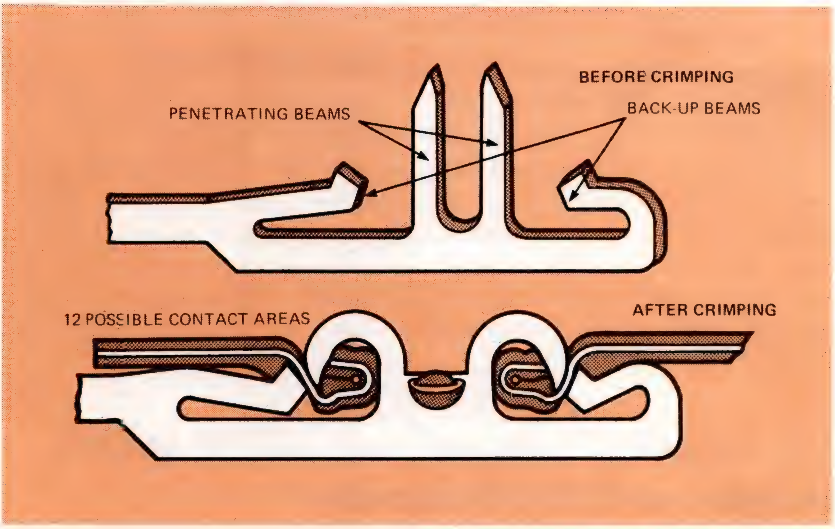


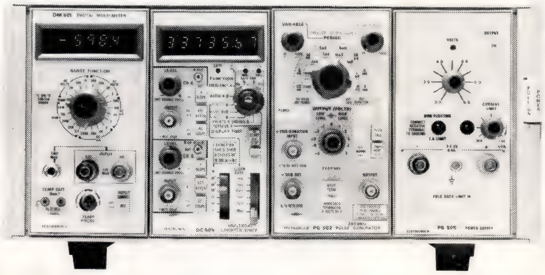
Fig. 1—Flattac connectors, shown in cross section, provide the kind of form factor connection that thin, flat-conductor cable should have—while still providing low contact resistance.

With a single semi-automatic operation, you get up to 35 simultaneous low-resistance electrically- and mechanically-sound crimped terminations. These can be flat cable to round wire, flat cable to post, or flat cable to board. No post-crimping strain relief is required.

Elco Corp., Willow Grove, PA 19090. Phone(215)659-7000.

Circle No. 143

If you design with ECL or TTL, You need to know about Tektronix TM 500



If You're into High Speed Logic,

the Tektronix TM 500 High Speed Logic Instrumentation plus the Tektronix 485 Oscilloscope (350 MHz) or 475 Oscilloscope (200 MHz) provide all the instrumentation you need for TTL or ECL up to 250 MHz. The four plug-ins of the TM 500 High Speed Logic system are a PG 502 Pulse Generator ($1195) with 1 ns rise time and independently variable logic 1 and 0 levels . . . a DC 505 Digital Counter ($1395) with 10 ns single shot resolution and averaging to 100 ps . . . A DM 501 Digital Multimeter ($550) with temperature measurement capability added to all its conventional functions (so you can verify operating temperatures of logic IC's and detect hot spots in tightly packed circuitry) . . . and the PS 505 Power Supply ($175) with the 3.0 to 5.5 V dc high-current (4 A) output essential for breadboarding or testing TTL and ECL devices. Also, you can expand the capabilities of the system to provide jitter-free oscilloscope triggering for viewing any segment of long pulse sequences by including the DD 501 Digital Delay ($495). The 485 Oscilloscope features dual trace, 1 ns rise time, and delayed sweep.

Whatever Pursuit in Electronics You're Into, you should learn more about TM 500 instrumention. A particular group of plug-in modules in a four-hole mainframe provides the instruments most often needed in telecommunications, another fulfills the needs of industrial instrumentation calibration and troubleshooting, another for medical instrumentation, others for education, and so on.

For more information Circle No. 32

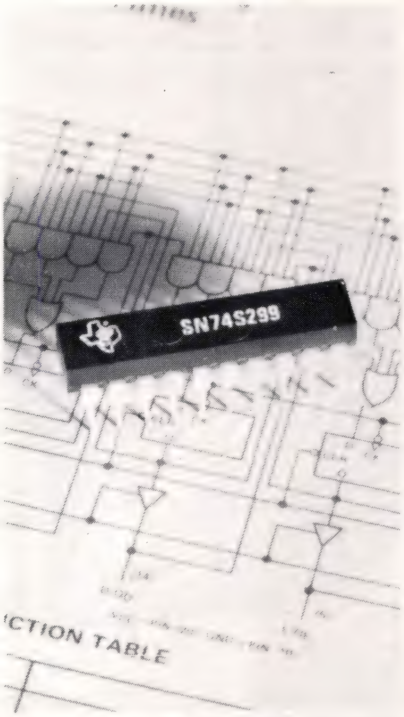
The TM 500 Concept,

TM 500 is a growing, compatible family of 29 plug-in modular instruments, accessories, and one, three, and four-hole mainframes providing the common power supply. *It's multifunctional:* The plug-ins include 11 signal sources, 5 counters, 2 digital multimeters, 5 power supplies, 3 signal processors, 1 oscilloscope, 1 X-Y monitor and even a blank plug-in kit, so you can assemble the specialized circuits you require. *It's versatile:* You can select from general-purpose instruments, such as the DM 501 Multimeter, or highly specialized instruments such as the TG 501 Time Mark Generator. You can select a system of instruments exactly tailored to your needs. *It's synergistic:* The instruments can "work together" through a common interface circuit board, so your lab bench needn't be cluttered with interconnecting cables. *And it's neatly configurable:* The TM 501 (one), TM 503 (three), and TM 504 (four-compartment) mainframes are attractive and compact. Since the typical four-instrument system only weighs about 20 pounds, it can be hand-carried as easily as it goes onto a bench. The TM 504 ($225) is only 11″ W x 6″ H x 20″ D. In rack mounting, each bay contains six instruments. And Tektronix SCOPE-MOBILE® carts let you put your entire instrumentation requirements on wheels.

Find Out What TM 500 Can Do For You. Get the new TM 500 Booklet A-3072 with full specifications and suggested package configurations, or contact your local Tektronix Field Engineer for a demonstration. Or write to Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077. In Europe, write Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands

TEKTRONIX®
committed to technical excellence

For a demonstration Circle No. 33



SCHOTTKY SHIFT REGISTER HAS PARALLEL ACCESS. Designed specifically to reduce pc board areas, the bidirectional SN74S299 operates at 70 MHz. Featuring multiplexed pnp inputs/3-state outputs, the device provides the equivalent of two 16-pin SN54S/74S194 or one 24-pin SN54/74198 in a single 20-pin package. With pin-row spacings of 0.3 in., the unit reduces board area by 40% and 55% when compared to two 16-pin or single 24-pin registers, respectively. The register is housed in a plastic DIP, and temp. range is 0 to 70°C. \$5.60 (100). Texas Instrument Inc., Box 5012, MS/308, Dallas, TX 75222. Phone(214)238-3741.
Circle No. 170

SOS IS ALIVE AND WELL IN RAM. This 1k RAM will be offered as an alternative to currently available high-dissipation bipolar memories. Production quantities will be stocked during the third quarter of 1975. Projected access time is approx. 120 nsec at 10V, with cycle times of 150 nsec. RCA Solid State Div., Box 3200, Somerville, NJ 08876. Phone(201)722-3200. **Circle No. 171**

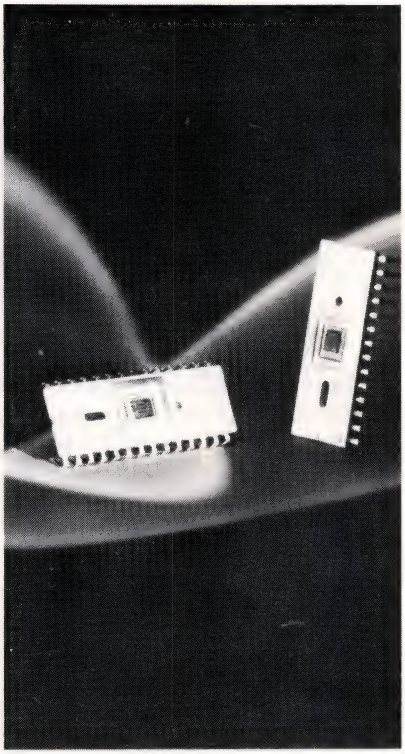
GAS-DISCHARGE DISPLAY DRIVER IS COMPATIBLE WITH MOS. This monolithic IC for driving high-voltage gas discharge displays is designed for Beckman or Burrough's Panaplex^{R} units. The circuit has 8 separate channels—one for each of the 7 display segments and an additional one for the decimal point. Min. breakdown is 80V. MC3491, in plastic, costs \$2.95 (25-99). Motorola Inc., Semiconductor Products Div., Box 20924, Phoenix, AZ 85036. Phone(602) 244-3464. **Circle No. 172**

BIPOLAR ROM OFFERED IN FULL MIL-TEMP. RANGE. Organized as 256 words by 4 bits/word, these programmable ROM's are designed for other TTL devices. 82S126 has open-collector outputs, while 82S129 has tri-state outputs. Read time is 35 nsec typ., 70 nsec max. over the temp. range of −55 to +125°C and ±10% V_{cc}. Both devices are supplied with all outputs at logical "0." Packaging is in 16-pin ceramic, \$24 (100). Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. Phone(408)739-7700.
Circle No. 173

ZENER DIODE LINE OFFERS WIDE RANGE OF BREAKDOWNS. Covering from 3.3 to 200V with a tolerance of ±5%, these zener diodes have currents as high as 4.8 mA for the upper voltage value and 276 mA for the lower value. BZY 97 line comprises silicon planar units in a DO-41 plastic case with axial connecting leads. Siemens Corp., 186 Wood Ave. South Iselin, NJ 08830. Phone(201)494-1000. **Circle No. 174**

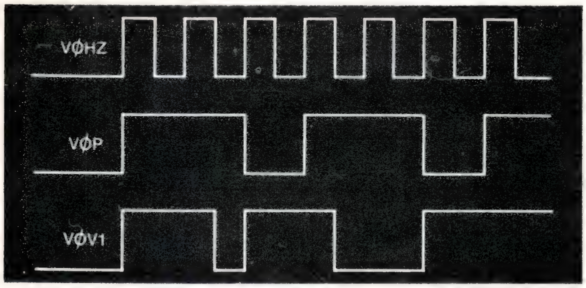
COMPLETE TV SOUND CHANNEL PACKED IN ONE IC. Contained in the TDA1190 are an IF amplifier/limiter, active low-pass filter, FM detector, dc volume control and power output amplifier. Output is typ. 4.2W@24V/16Ω and limiting is typ. at 30 μV. The unit has no thermal feedback and no radiated frequencies are generated, thus minimizing the need for shielding. \$2.80(100-999). SGS-ATES Semiconductor Corp., 435 Newtonville Ave., Newtonville, MA 02160. Phone(617)969-1610.
Circle No. 175

RED DISCRETE LED HAS EXTRA-HIGH INTENSITY. Mechanically identical to the MV5050, the device is constructed from gallium-arsenide phosphide and offers a 2.5× intensity improvement. MV5753 projects a 65° beam angle, while MV5754 has a 24° beam angle. Max. power dissipation is 105 mW and max. continuous forward current rating is 35 mA at 25°C. Intensities of 4 and 8 mcd typ.@20 mA are reached in MV5753 and MV5754, respectively. 89¢(100-999). Monsanto Commercial Product Co., 3400 Hillview Ave., Palo Alto, CA 94304. Phone(415)493-3300. **Circle No. 176**



NONLATCHING 16-CHANNEL MULTIPLEXER OFFERED IN CMOS. The IH5060 is a plug-in replacement for the DG506 and HI506. Housed in a 28-pin DIP, it is available in both a MIL-temp (−55 to 125°C) and a commercial (0 to 70°C) model. Max. negative and positive supply current drain for the mil model is 300 μA (2 mA for the comm. model). \$28 comm. version or \$55 mil version. Intersil Inc., 10900 N. Tantau Ave., Cupertino, CA 95014. Phone(408)257-5450. **Circle No. 177**

Creating Waveshapes to Test Charge Coupled Devices? Digital Arrays?



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- Clock Source • Width/Delay Control
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Call collect or write for our magnetic tape and CCD Technology Notes.

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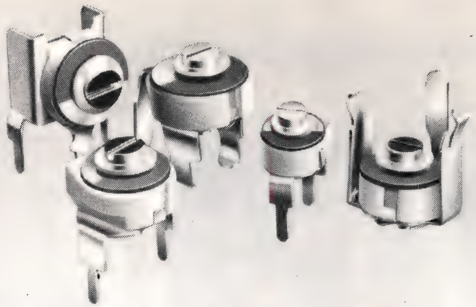
For more information, Circle No. 34



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These rotary ceramic disc trimmer capacitors are perfect for broadband applications from audio to 500 MHz. They provide an ideal low cost means of "trimming" circuitry such as crystal oscillators, CATV amplifiers and all varieties of communication and test equipment.

These capacitors are available in three adjustment configurations: top tuning, side tuning for "in rack" adjustment and bottom tuning for "thru the board" adjustment. Three mounting configurations allow drop in replacement for other types of units.

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For more information, Circle No. 35

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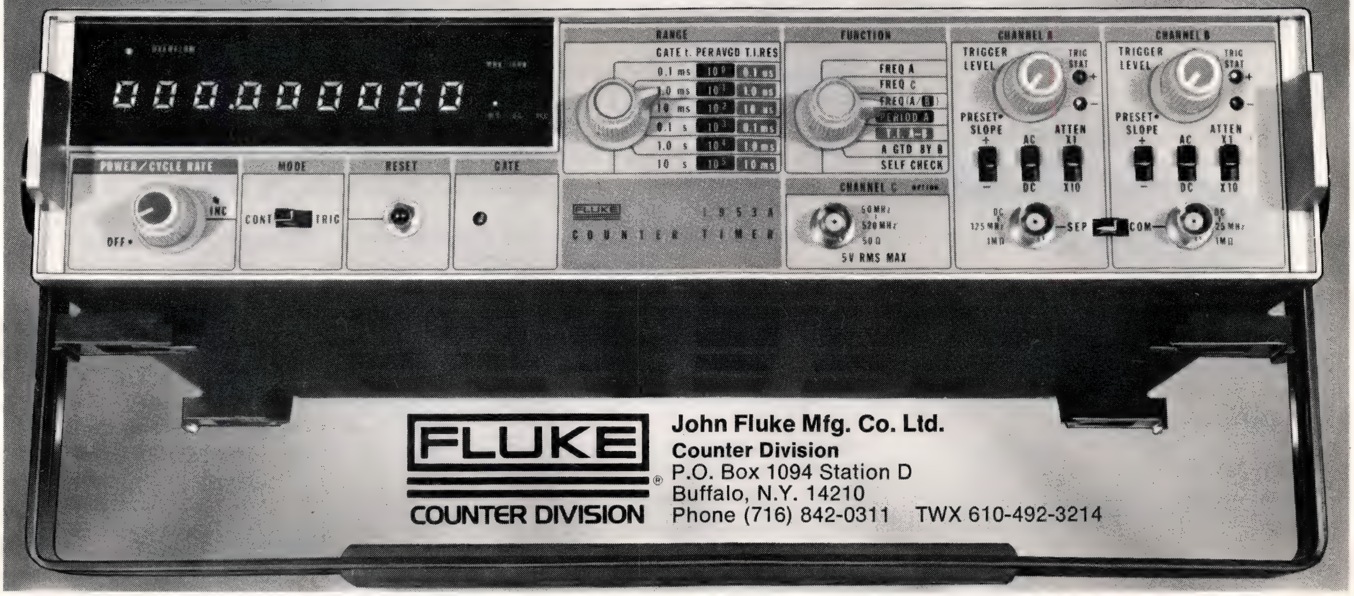
One of Fluke's 'New Breed' of powerful LSI/MOS counters

$849

U.S. price F.O.B. Buffalo, N.Y.
Remote programming and other options extra.



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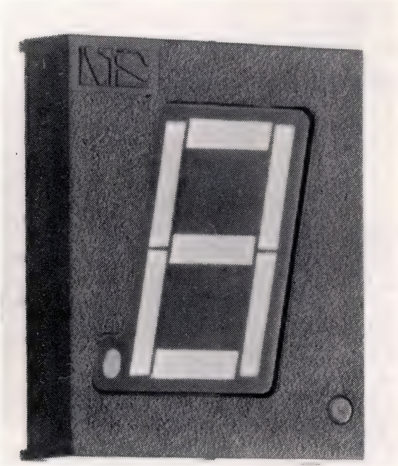
For a demonstration Circle No. 18

For more information Circle No. 44



LARGEST LED DISPLAYS PERMIT 25-FT READING DISTANCE. These 2/3-in. units are claimed to be the largest 7-segment, red, single-digit GaAsP displays available. Both offer broad stroke width for extended viewing ease, and typical luminous intensity of 5 mcd@20 mA (I_F). Both the NSN61L (common cathode, right-hand decimal) and NSN64R (common anode, left-hand decimal) cost $2.75 (1000). National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051. Phone(408)732-5000.

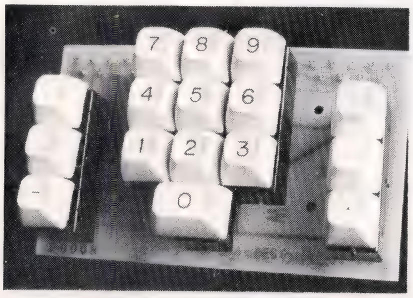
Circle No. 178

CURRENT-SENSITIVE RELAY DRIVES DIRECTLY FROM DTL OR T^2L. Designated R10S, this relay is available with 1, 2, 3 and 4 Form C contacts in ratings from dry circuit to 3A at 28V dc, resistive. There is a choice of pc-board, solder or octal-type termination. Maximum pick-up for a 1 Form C model with 1000Ω coil is 2.3 mA. Contact-life expectancy is 100,000 operations at full load. With solder or pc termination the R10S measures 1.5×0.735×1.165-in., and weighs as little as 22 grams. Potter & Brumfield Div. of AMF Inc., Princeton, IN 47670. Phone(812)385-5251.

Circle No. 179

ELAPSED-TIME INDICATORS MEET MIL-SPEC REQUIREMENTS. Operating from a 5V regulated source, the MS 90386 occupies a panel area of <0.5 $in.^2$, has a depth of 0.2 in. and weighs <2 grams. Power consumption is below 25 µW. Models are available for above-panel and below-panel mounting and with 1000 and 5000-hr. time scales. <$10 in moderate production quantity. Curtis Instruments, Inc., 200 Kisco Ave., Mt. Kisco, NY 10549. Phone(914)666-2971.

Circle No. 180



WIRED-ONLY KEYBOARD HAS 10 ADDER AND 6 FUNCTION KEYS. Nonencoded, this 16-key unit features 0.17-in. key-stroke travel and uses an environmentally-immune reed switch. It features 2-shot molded keytops, low-cost pc board mounting, turret connectors and a 5-yr. warranty on the reed switch. Under $20 in OEM quantities. Key Tronic Corp., Bldg. 14-Spokane Industrial Park, Spokane, WA 99216. Phone(509)928-8000. **Circle No. 181**

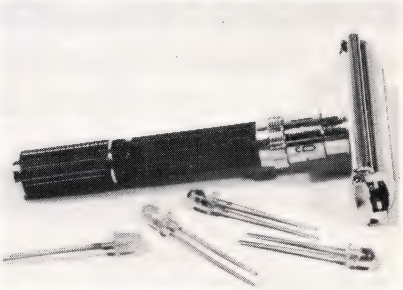
LATCHING RELAY HANDLES UP TO 1/3-H.P. 120V AC MOTOR. The 32-series single coil ac or dc mechanical latching memory relay provides remote or sequence control for commercial and industrial applications. Standard silver cadmium-oxide 1pdt or 2pdt contacts have a rating of 10A, 24V dc/120V ac, 50-60 Hz. Nominal operating voltages range from 6 to 110V dc or 6 to 140V ac. Relay life is rated at 50,000 operations. 6V dc spdt $5.68 (50). North American Philips Controls Corp., Frederick, MD 21701. Phone(301)663-5141.

Circle No. 182

MERCURY TIP-AND-TILT SWITCH CARRIES 0.5A/120V AC RATING. Smaller than a dime, it measures 0.222 in. diameter by 0.375 in. high. Price, in high volume, drops to 6¢ (samples are available for 10¢ each). Durakool, Inc., 1010 N. Main St., Elkhart, IN 46514. Phone(219)264-1116. **Circle No. 183**

COMPACT OPTO-COUPLERS OFFER 0.5 pF ISOLATION CAPACITANCE. The JEDEC-registered 4N25, 4N26, 4N27 and 4N28 consist of a gallium-arsenide LED optically coupled to a silicon phototransistor. Minimum isolation voltages are 500V (4N28), 1500V (4N26, 4N27) and 2500V (4N25). Collector output current for the 4N25 and 4N26 is 10 mA typ.—for the 4N27 and 4N28, 1 mA min. Bandwidth for all is 150 kHz typ. $1.70, $1.40, $1.15 and 95¢, respectively (100). National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051. Phone(408)732-5000.

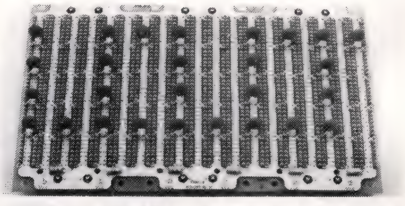
Circle No. 184



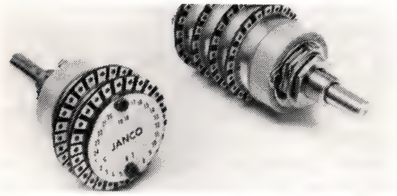
YELLOW LED LAMPS GLOW BRIGHTLY, COST LITTLE. These clear yellow (521-9204) or diffused yellow (521-9205) gallium-phosphide lamps have luminous intensity of 2 mcd and wide viewing angle. The package is T-1-3/4. 55¢ each (1000). Dialight, 203 Harrison Pl., Brooklyn, NY 11237. Phone(212)497-7600.

Circle No. 185

IMMERSION-SEALED CERMET TRIMMERS HANDLE 0.5W. The 3/8-in. sq. single-turn Type E is offered with values from 10Ω to 2 MΩ at ±10% tolerance. A multi-finger contact eases adjustment. Operating range is −55 to +125°C, with a TC of 100 ppm/°C over the entire range. <50¢ in production quantities. Allen-Bradley Co., 1201 S. Second St., Milwaukee, WI 53204. Phone(414)671-2000. **Circle No. 186**



CIRCUIT BOARDS PACK MORE VOLTAGE AND GROUND PLANES/$IN.^2$. Series MD boards come with or without decoupling capacitors—either ceramic or tantalum. They are available either wire-wrapped for assembly, or unwrapped for prototype production. Options include committed or noncommitted power and ground planes; laminated bus bars for additional noise suppression; and contact pins in lengths for 1-, 2-, or 3-level wire wrapping. Garry Mfg. Co., 1010 Jersey Ave., New Brunswick, NJ 08902. Phone(212)545-2424. **Circle No. 187**



COMPACT DRY-CIRCUIT ROTARY SWITCHES TAKE A BOW. The 3100-series switches are available in a variety of detent angles and output codes. Detent angles range from 15 to 45°, while output codes range from straight decimal to octal and hexadecimal, with and without complements and parity bits. Basic switch length is <1 in. and additional decks add approx. 5/16 in. each. All switching parts are hard gold-plated and treated for "dry" circuit service. Janco Corp., 3111 Winona Ave., Burbank, CA 91504. Phone(213)845-7473.

Circle No. 188

MINI-NOISE COAX CABLE IMPROVES NOISE REDUCTION BY 250%. Particularly well suited to applications such as high-gain audio amps, scope probes, photo cells, accelerometers and magnetic recording heads, the X4 cable has 50Ω impedance and 30 pF/ft capacitance. 26.7¢/ft (10,000 ft). Malco, a Microdot Co., 200 Pasadena Ave., S. Pasadena, CA 91030. Phone(213)682-3351.

Circle No. 189

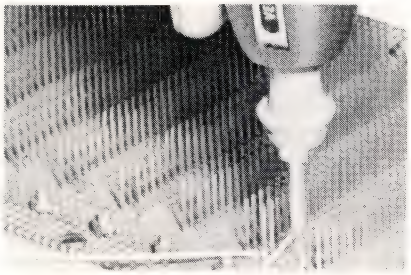
STRAIN-RELIEF BUSHING MEETS INTERNATIONAL REQUIREMENTS. USR-3 and USR-4 nylon bushings are now available for 0.256- to 0.4-in. dia. cords. They hold insulated cords and cables according to requirements of IEC 335, CEE 10 & 11, VDE 720 & 730 and BS13456. The bushing can be securely fastened to a chassis and need not be unfastened or removed for cord removal or replacement. Its ratchet cord lock can be set with a plier, released with a screw driver. Heyman Mfg. Co., N. Michigan Ave., Kenilworth, NJ 07033. Phone(201)245-2345.

Circle No. 190

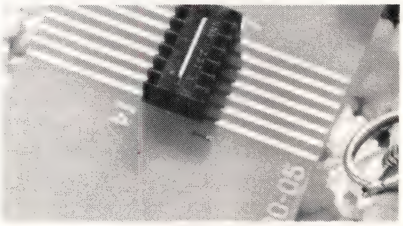
MINIATURE 5A/240V AC RELAY HAS UL, CSA AND VDE LISTING. These industrial relays occupy as little as 1.2 $in.^3$, yet control up to 5A for 4 C, 7A for 2 C, and 10A for 1 C at 240V ac resistive loads. Life expectancy exceeds 10^8 mechanical operations. Coil voltages range from 6 to 240V ac or 6 to 110V dc. Contacts are gold-flashed silver-cadmium oxide, with 1 to 10A ratings depending upon relay type. From $2 to $6. Arrow-M Corp., 250 Sheffield St., Mountainside, NJ 07092. Phone(201)232-4260. **Circle No. 191**

4PDT INDUSTRIAL RELAY ENDS 3-POLE LIMIT FOR 10A UNITS. All 4 poles of the Frame 284 have full-load switching capability, provided the total load is within the 30A limit. Flat, male quick-connect 0.187-in. terminals plug into companion sockets, but also are pierced to accommodate solder connections. Standard units are enclosed in clear, polycarbonate covers. $6.75 (100). Struthers-Dunn, Inc., Lambs Rd., Pitman, NJ 08071. Phone(609)589-7500.

Circle No. 192

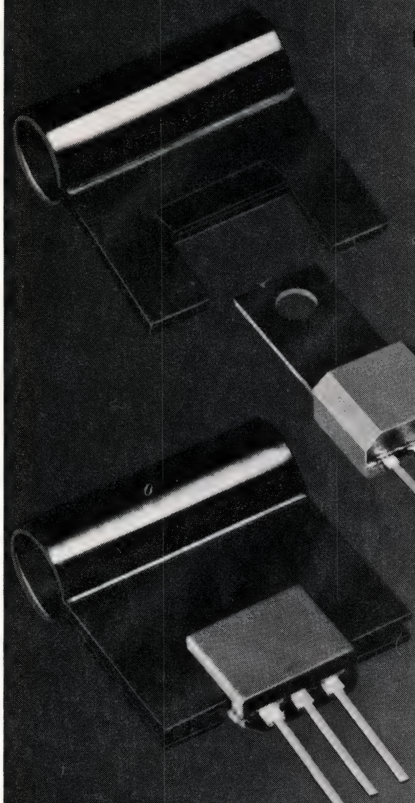


BATTERY OPERATED WRAPPED-WIRE TOOL SELLS FOR $59.69. The 9-oz. P160-4 tool with P160-2 wrapping bit wraps 0.025- to 0.028-in. sq. posts with 26- to 30-ga. wire. Its 0.070-in. bit radius allows wrapping of posts spaced on 0.10-in. centers. A nickel-cadmium battery (furnished) powers it for 8 hrs., recharges in 14-16 hrs. with the charger provided. Vector Electronic Co., Inc., 12460 Gladstone Ave., Sylmar, CA 91342. Phone(213)365-9661. **Circle No. 193**



SOLDERLESS PRESS-ON IC SOCKET MAKES HIGH-PRESSURE CONTACTS. The Popit™, for use with single or double-sided pc boards, is manufactured of glass-filled polyester thermoplastic and contains contacts of spring-copper alloy. It requires only 2 holes to mount. The wiping-action contacts provide 250-gram contact pressure and 25 mΩ contact resistance at 1A. Continuous operating temperature is −55 to +85°C. Cannon Electric Div., 666 E. Dyer Rd., Box 929, Santa Ana, CA 92702. Phone(714)557-4700.

Circle No. 194



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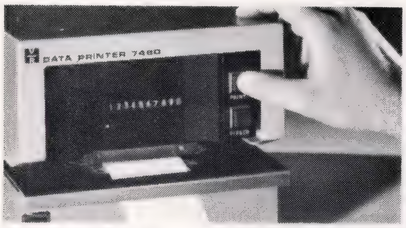
EQUIPMENT

FREQUENCY SYNTHESIZERS COVER 0.01 Hz TO 100 kHz, 1 MHz. Designated PM 5141 and PM 5142, these sine/square wave instruments can be fitted with a programmable-operation option. Frequency is set by 4 thumbwheel switches and 5 range push-buttons. Both models deliver 5V into 600Ω and this can be attenuated to 5 mV. The optional remote control for range and frequency can be fitted by the user. $725 and $830. Philips Test & Measuring Instruments, Inc., 400 Crossways Park Dr., Woodbury, NY 11797. Phone(516)921-8880.

Circle No. 195

POCKET CALCULATOR WITH MEMORY HOLDS THE PRICE LINE. Priced at $39.95, the 4-function CAMBRIDGE/MEMORY features click-action keys, 8-digits and floating decimal. Four alkaline AAA 1.5V batteries power it for 25 hrs. of use. FP Model & Co., Inc., 37 Riverside Dr., New York, NY 10023. Phone(212)362-5141. **Circle No. 196**

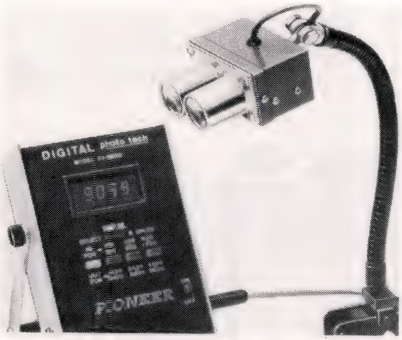


MILLION-PRINTOUT DATA PRINTER PRODUCES 1 10-CHAR. LINE/SEC. In the Series 7480, each character is selected by the 4-bit binary code parallel input signal from the 16 characters available on each standard wheel. The printer input circuitry is compatible with both DTL and TTL logic. Character style may be either modified bold or OCR, and electronic multiplexing is utilized throughout for max. reliability. Veeder-Root, Digital Systems Div., 70 Sargeant St., Hartford, CT 06102. Phone(203)527-7201.

Circle No. 197

STROBE-TACH INCORPORATES INTEGRAL FLASH DELAY CONTROL. This portable, 100% solid-state unit can stop the motion of moving objects. The built-in position control lets you inspect moving objects at any desired point in the motion cycle. Model 910 also can be used as a tachometer with 4 ranges covering up to 30,000 RPM with accuracy of 1-1/2% of P.S. $425. Power Instruments Inc., 7352 N. Lawndale Ave., Skokie, IL 60076. Phone(312)676-7600.

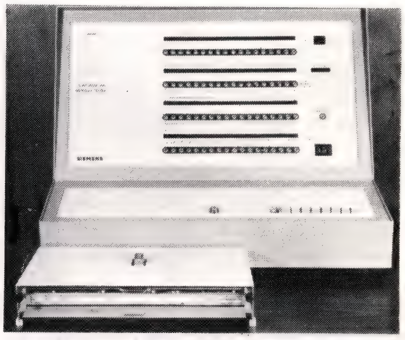
Circle No. 198



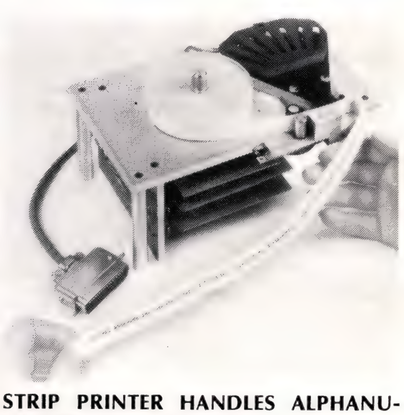
PHOTOCELL DIGITAL TACH MAKES TOUCHLESS MEASUREMENTS. Powered by rechargeable batteries, the 2-component Model DT 9600 has a crystal time base for stability. The operating ranges are 150-300, 300-600, 600-1200, 1200-2400, 2400-4800 and 4800-9600 RPM. Readout is on a LED display. Pioneer Electric & Research Corp., 743 Circle Ave., Forest Park, IL 60130. Phone-(312)771-8242. **Circle No. 199**

VOLTAGE BREAKDOWN TESTER HELPS MEET UL REQUIREMENTS. Model P-2B consists of an adjustable ac high-voltage source with voltmeter in the output circuit, and a breakdown indicator. An integral dc high-voltage source suitable for flash-testing capacitors and insulating materials is also provided. Beckman Instruments, Cedar Grove Operations, 89 Commerce Rd., Cedar Grove, NJ 07009. **Circle No. 200**

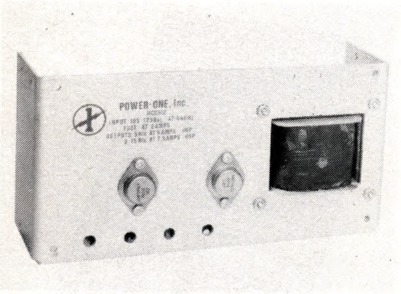
COMPUTER OPERATED SCREWDRIVER IS A REALITY. A computer-operated screwdriver is now available with interface and software for D.E.C. PDP/8 computers and the COLT test language. In addition, the screwdriver servo system is available as a separate subsystem for applications where the computer is not available or needed. Under computer control are reference value, servo gain, and servo sense. Optimized Devices, Inc., 220 Marble Ave., Pleasantville, NY 10570. Phone (914)769-6100. **Circle No. 201**



INTERFACE MODULES PERMIT HIGH-SPEED MEMORY TESTS. The modules attach to the Computest Model 901 semiconductor memory tester and contain all of the necessary device electronics for interfacing the 901 to the memory under test. A pROM holds the device programming information. Device timing, test sequence and test data pattern are automatically programmed. From $700 to $1500. Siemens Corp., 3 Computer Dr., Cherry Hill, NJ 08002. Phone(609)424-2400. **Circle No. 202**



STRIP PRINTER HANDLES ALPHANUMERICS AT 50 CHAR./SEC. The device prints on a strip of 1/2-in. wide pressure-sensitive paper. The DX506 is comprised of the MPH-1 matrix print head, the CC64 character-generator module, the AC64 amplifier module and the paper-drive logic module. In the print head, vertical solenoid-driven pins produce a character when the paper is advanced past them. Amperex Electronic Corp., Hicksville, NY 11802. Phone-(516)931-6200. **Circle No. 203**



TWO OEM POWER SUPPLIES SUIT T²L/DTL AND CMOS NEEDS. Each features a 5V output with overvoltage protection and a separate 9 to 15V adjustable output. Line/load regulation is 0.02%, current foldback is built-in, and both are full rated to 50°C. Output rating on model HBB512 is 5V@ 3A and 9 to 15V @ 1.25A; on model HCC512, 5V@ 6A and 9 to 15V@ 2.5A. $54.95 and $86.95 (1-9). Power-One Inc., 531 Dawson Dr., Camarillo, CA 93010. Phone(805)484-2806. **Circle No. 204**

SINE/SQUARE-OUTPUT SYNTHESIZER COVERS 0.1 Hz TO 13 MHz. The 5-digit Model 1013 features a metered, leveled sine wave output up to 3V, controlled by a precision output attenuator adjustable in 10 dB steps from 0 to 90 dB plus continuous level control. Harmonic distortion is below 50 dB from 0.1 Hz to 1 MHz and 40 dB from 1 to 13 MHz. The square-wave output drives 50Ω and TTL logic. $1595. Comstron Corp., 120-30 Jamaica Ave., Richmond Hill, NY 11418. Phone(212)441-3200. **Circle No. 205**

CLAMP-ON SERVICE TESTERS READ AC CURRENT IN SEC. All 3 models of AMP-CLAMP^R (Model 294A, 295 VA and 296 VOA) read current in 5 ranges from 0-6 to 0-300A. Model 295 VA and 296 VOA also have 4 voltage ranges from 0-30 to 0-600V rms, and Model 295 VOA has an added 0-500Ω range. A finger-operated lever permits clamping the dial pointer for convenience of use. $45, $53 and $71.50, including test leads and instructions. Simpson Electric Co., 853 Dundee Ave., Elgin, IL 60120. Phone-(312)697-2260. **Circle No. 206**

COMPACT DIGITAL TACH SENSES VIA MAGNETIC PICKUP. The ac-operated Model 1700 reads out on 4 half-in. LED digits and displays a nonblinking reading from 1 to 9999 RPM. Its magnetic pickup senses the rotating speed of an existing (or added) steel gear with 30 to 144 teeth (60 teeth standard). $195. Power Instruments, Inc., 7352 N. Lawndale Ave., Skokie, IL 60076. Phone(312)676-2300. **Circle No. 207**

DIGITAL TRANSMISSION MM DIAGNOSES PHONE-CIRCUIT ILLS. The Model 430 "multimeter" combines the functions of frequency counter, noise and level test set, capacitance bridge and decade box with standard voltmeter functions. Signal level and noise are displayed digitally. $1395. Wavetek, Box 651, San Diego, CA 92112. Phone(714)-279-2200. **Circle No. 208**

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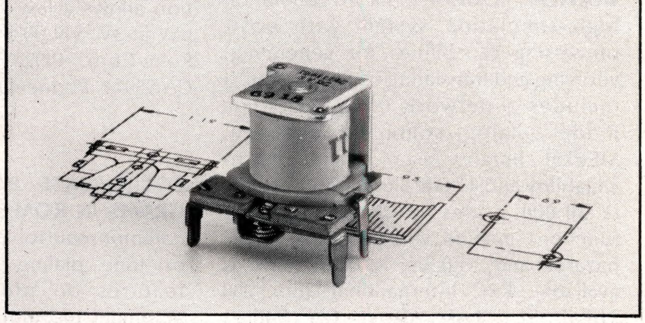

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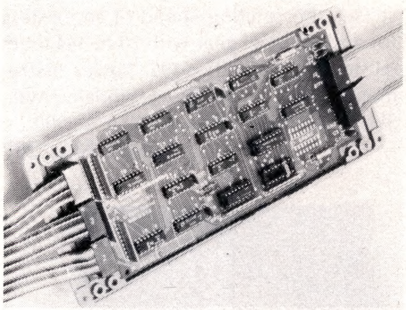
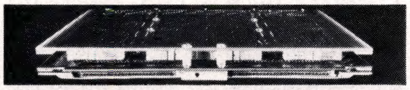


SMART CABLES AND PC BOARD COMPRISE I/O INTERFACE. This system uses a single half-card—called an I/O Distributor (not shown)—and a set of intelligent, computer-driven cables containing a PicoProcessor™ (shown), to allow any CAI LSI computer to communicate with up to 8 parallel or serial devices. The I/O Distributor provides interrupt processing, clocks and buffering. Each intelligent (ribbon) cable interfaces to a PicoProcessor imbedded in the cable near the peripheral. These fast compact processors are microcoded for the characteristics of the desired device. I/O Distributor is $380; cables cost $145 each. Computer Automation Inc., 18651 Von Karman Ave., Irvine, CA 92664. Phone(714)833-8830. **Circle No. 209**

SOFTWARE SIMPLIFIES NETWORK SIMULATION. LOGCAP-2 is a 3rd generation logic-simulation system with post-processing capabilities for generating, verifying and translating test programs. It includes a network compiler, logic model catalog, command language, MSI/LSI library, user library, macro capability and 4-state simulator. Capacity is 30,000 nodes. Built in checking functions include verification of races, hazards and toggles. A user guide is available. RRC International, Inc., 200 Third St., Los Altos, CA 94002. Phone(415)948-0877. **Circle No. 210**

NEED A CALCULATOR? BUILD IT YOURSELF. This do-it-yourself kit version of the Sinclair Scientific calculator measures 4-3/8×2×11/16 in. and weighs only 3-3/4 ozs. Twelve functions are provided using Reverse Polish logic with post-fixed operators. Entries and results are in scientific notation with a signed 5-digit mantissa and a 2-digit exponent ($10^{\pm 99}$). The kit takes 3 hrs. to build and has a 1-yr. guarantee. $49.95. FP Model & Co., Inc., 37 Riverside Dr., New York, NY 10023. Phone(212)362-5141. **Circle No. 211**

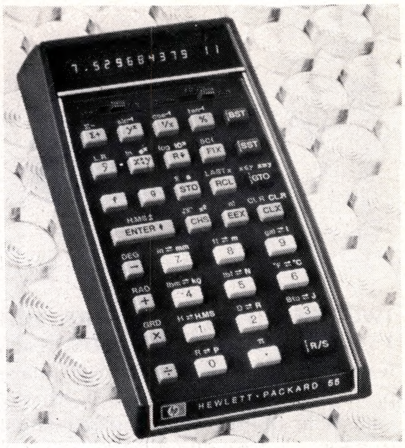
GRAPHICS GENERATOR SYSTEM FITS ON SINGLE PC CARD. Model 4416 graphics video generator I/O card produces a composite video signal which displays a 256×256 point matrix on standard TV monitors. Designed for the HP 2000 series computers, the card provides software drivers for the HP operating system. Local screen refresh is implemented with 4k RAM's, allowing a point transfer rate of >200 kHz. $2750. Delivery is 60 days ARO. Intermedia Systems, 20430 Town Center Lane, Cupertino, CA 95014. Phone(408)996-0900. **Circle No. 212**



ULTRA-RUGGED 8k RAM RUNS IN HEAT OR COLD. Designed to meet MIL specs, Model 2032 RAM will operate over a range of −55 to +95°C. The memory module features static memory that needs no refreshing. CMOS construction allows a low standby current of 25 μW at 3V. $11,000. Delivery is 150 days. Rolm Corp., 18922 Forge Dr., Cupertino, CA 95014. Phone(408)257-6440. **Circle No. 213**

SOLID-STATE PABX STORES PROGRAMS IN ROM'S. The fully electronic common-control EBX 60/100 offers pulse or tone dialing plus all well-known features on plug-in pc cards. An automatic test unit plugs into the cabinet providing complete system test and maintenance capabilities. Digital display in the attendant's console indicates call status. Norelco, 91 McKee Dr., Mahwah, NJ 07430. Phone(201)529-3800. **Circle No. 214**

ARITHMETIC UNIT BOOSTS NOVA 2'S SPEED. Model 279-0 is a high-speed multiply/divide/shift unit, packaged on a 15×15-in. board that plugs into slot 2 of the Nova 2. It multiplies in 5.5 μsec, divides in 5.8 μsec, and performs 13 shift operation in 2.2 to 8.5 μsec (single and double accumulator, 0 to 31 bit positions). $1400. Unitech, Inc., 1005 East St. Elmo Rd., Austin, TX 78745. Phone(512)444-0541. **Circle No. 215**



HP-55 CALCULATOR BOASTS EVEN MORE OF THE SAME. This 9-oz. calculator offers 49 steps of program memory, 86 keyboard functions and 20 addressable memories. Also featured is a built-in digital timer accurate to ±0.01%, with the ability to store and recall up to 10 time intervals. $395. Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, CA 94304. Phone(415)493-1501. **Circle No. 216**

GRAPHICS TERMINAL ELIMINATES COMPUTER OVERHEAD. The Dynagraph system features hardware vector and char. generation with internal storage for 4k vectors, and char., command and display storage for 64k addressable locations. A data input rate of 250 kHz allows a flicker-free raster display. The command structure enables single instruction control of picture sets and separate control of multiple picture sets. Nuclide Corp., 642 E. College Ave., State College, PA 16801. Phone(814)238-0541. **Circle No. 217**

ORALLY OPERATED SYSTEM MAKES "OPEN SESAME" A REALITY. Voice-command system Model 400 converts acoustic inputs to digital code. With proper interfacing, the code can be used to enter data into a computer, retrieve stored info., or control machine operation. The system has a repertoire of 45 one-sec commands that are trainable on line. Options include 1000-wd. vocabulary, multi-word sentence recognition and voice response. Scope Electronics Inc., 1860 Michael Faraday Dr., Reston, VA 22090. Phone(703)471-5600. **Circle No. 218**

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Pull-Up
- Power Gate
- Open Collector
- Parallel
- "Wired OR"
- MOS Memory
- TTL Unused Gate
- Power Driver

Pull-Down
- ECL Output
- TTL Input
- MOS Memory

Other Applications:
- Impedance Balancing
- Current Limiting
- Line Termination
- Pulse Squaring
- TTL to ECL Translator

Check this cross reference chart

DALE	BECKMAN	CTS
LDP14-02-XXXG	899-1-RXXX	760-1-R
LDP14-01-XXXG	899-3-RXXX	760-3-R
LDP16-02-XXXG	898-1-RXXX	761-1-R
LDP16-01-XXXG	898-3-RXXX	761-3-R

Phone 402-371-0080 for complete price & delivery details.

DEPENDABLE DALE®

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